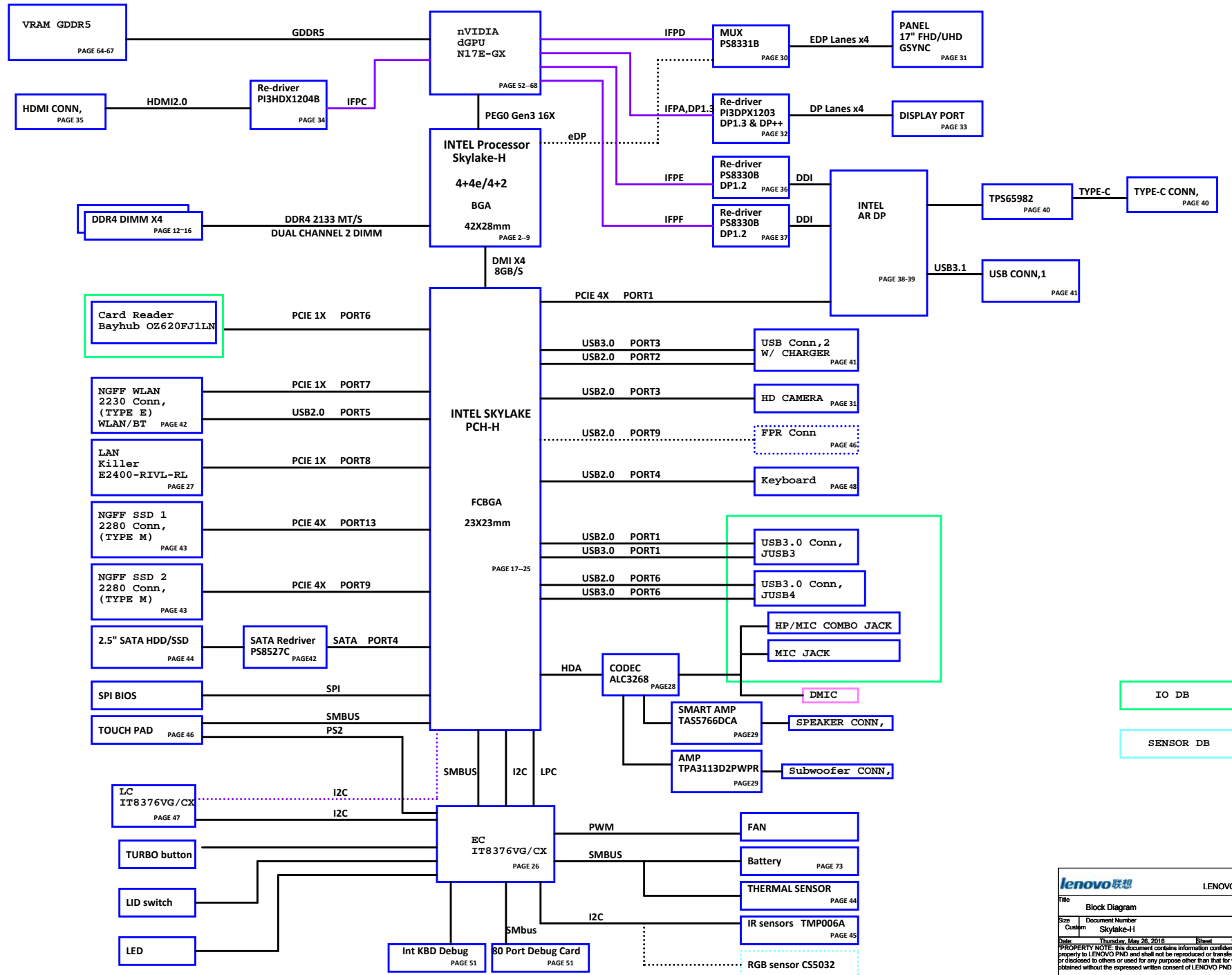


Schematic Block Diagram



PCIE Reversed

SKYLAKE_HALO
BGA1440

U1C

PCIE Reversed

dGPU PEG

dGPU PEG

BRD Note:
W=12mils;S=15mils;L<=400mils

+VCCIO

18 DMI_IT_MR_0_DP >>> D8 DMI_RXP[0]
18 DMI_IT_MR_0_ON >>> E8 DMI_RXN[0]
18 DMI_IT_MR_1_DP >>> E6 DMI_RXP[1]
18 DMI_IT_MR_1_ON >>> F6 DMI_RXN[1]
18 DMI_IT_MR_2_DP >>> D5 DMI_RXP[2]
18 DMI_IT_MR_2_ON >>> E5 DMI_RXN[2]
18 DMI_IT_MR_3_DP >>> J8 DMI_RXP[3]
18 DMI_IT_MR_3_ON >>> J9 DMI_RXN[3]

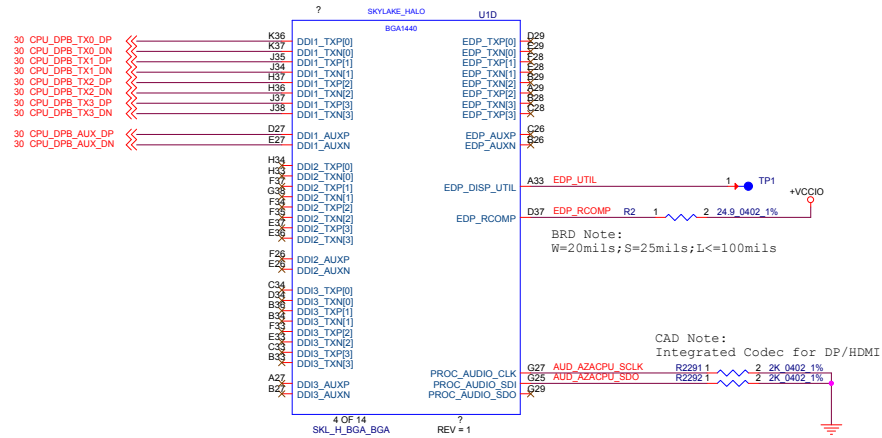
B8 DMI_TXP[0]
A8 DMI_TXN[0]
C6 DMI_TXP[1]
B6 DMI_TXN[1]
B5 DMI_TXP[2]
A5 DMI_TXN[2]
D4 DMI_TXP[3]
B4 DMI_TXN[3]

18 DMI_MT_IR_0_DP 18
18 DMI_MT_IR_0_ON 18
18 DMI_MT_IR_1_DP 18
18 DMI_MT_IR_1_ON 18
18 DMI_MT_IR_2_DP 18
18 DMI_MT_IR_2_ON 18
18 DMI_MT_IR_3_DP 18
18 DMI_MT_IR_3_ON 18

3 OF 14
SKL_H_BGA_BGA REV = 1

lenovo联想		LENOVO.CRDN	
File			
PROCESSOR-PEG/DMI			
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C	Skylake-H	v0.3	
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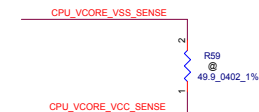
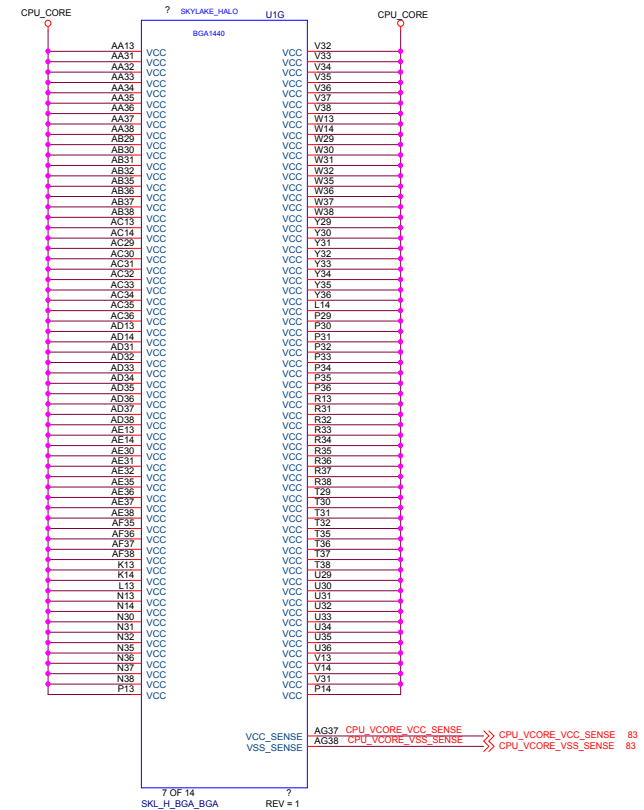
DDI B TO DP PORT, FOR DEBUG

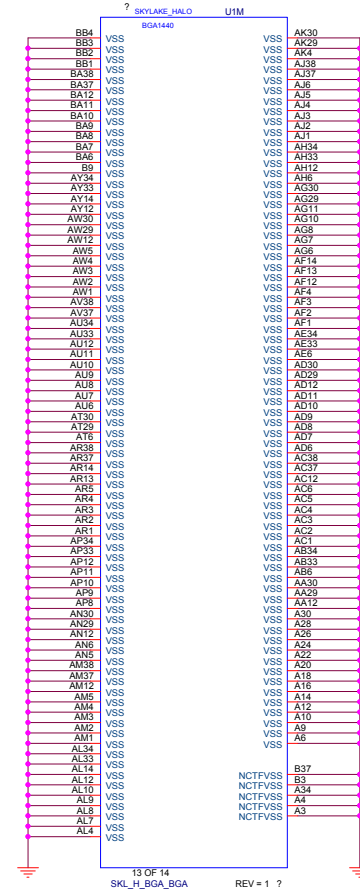
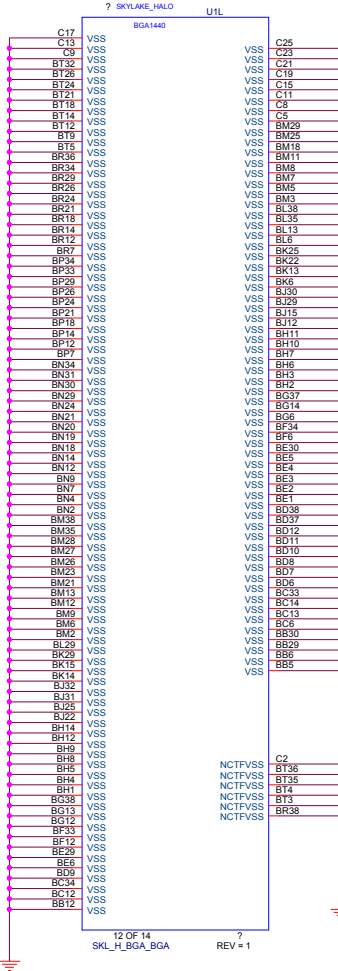
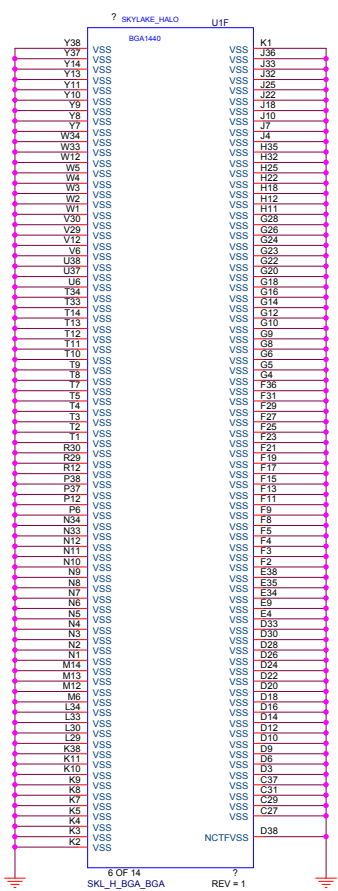


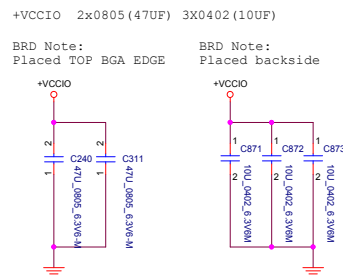
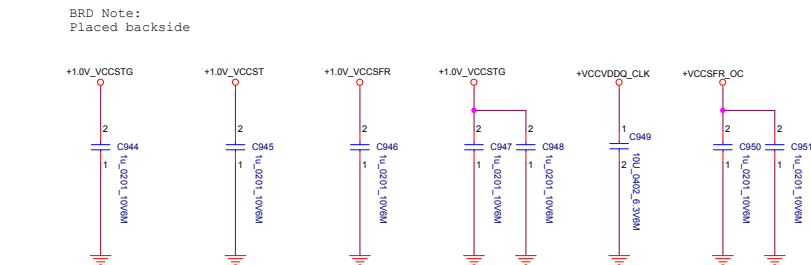
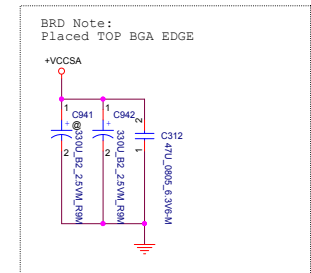
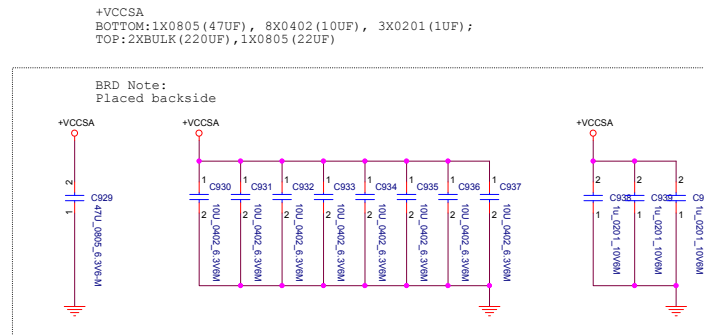
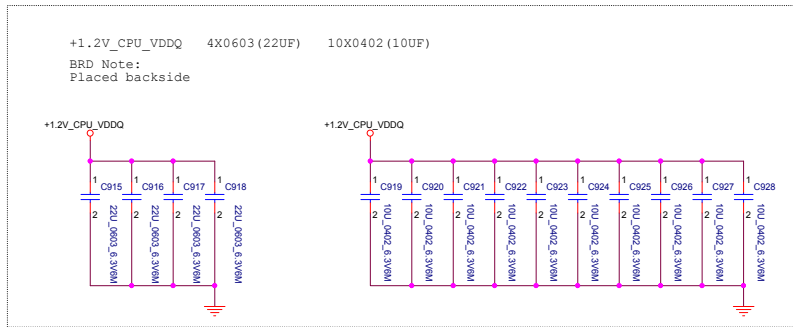
FOR H4+4e

SKYLAKE_HALO U1J	
BGA1440	
BJ17	VCCOPC
BJ19	VCCOPC
BJ20	VCCOPC
BK17	VCCOPC
BK19	VCCOPC
BK20	VCCOPC
BL16	VCCOPC
BL17	VCCOPC
BL18	VCCOPC
BL19	VCCOPC
BL20	VCCOPC
BL21	VCCOPC
BL22	VCCOPC
BM17	VCCOPC
BN17	VCCOPC
BJ23	RSVD
BJ24	RSVD
BJ25	RSVD
BK23	RSVD
BK24	RSVD
BK25	RSVD
BL23	RSVD
BL24	RSVD
BL25	RSVD
BL26	RSVD
BL27	RSVD
BL28	RSVD
BM23	RSVD
BL15	VCCOPC_SENSE
BN16	VSSOPC_SENSE
BL22	RSVD
BN22	RSVD
BP15	VCCEOPIO
BR16	VCCEOPIO
BT17	VCCEOPIO
BP16	RSVD
BR17	RSVD
BT18	RSVD
BN15	VCCEOPIO_SENSE
BN16	VSSOPIO_SENSE
BP17	RSVD
BN17	RSVD
BM14	VCC_OP1_P8
BL14	VCC_OP1_P8
BJ16	RSVD
BJ18	RSVD
AT13	ZVM#
AW13	MSM#
AU13	ZVM2#
AY13	MSM2#
BT29	OPC_RCOMP
BR26	OPCE_RCOMP
BP26	OPCE_RCOMP2

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SKL_H_BGA_BGA REV = 1







lenovo 联想		LENOVO.CRDN	
File			
PROCESSOR Decoupling 1/2			
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[illegible]

BRD Note:
Placed TOP BGA EDGE

WVCOT

C1185 330U, BE, 2.5VH, R5M

C1186 100U, BE, 2.5VH, R5M

C1187 330U, BE, 2.5VH, R5M

C1188 100U, BE, 2.5VH, R5M

C1189 47U, 006K, 6.3V6K

C1190 47U, 006K, 6.3V6K

C1191 47U, 006K, 6.3V6K

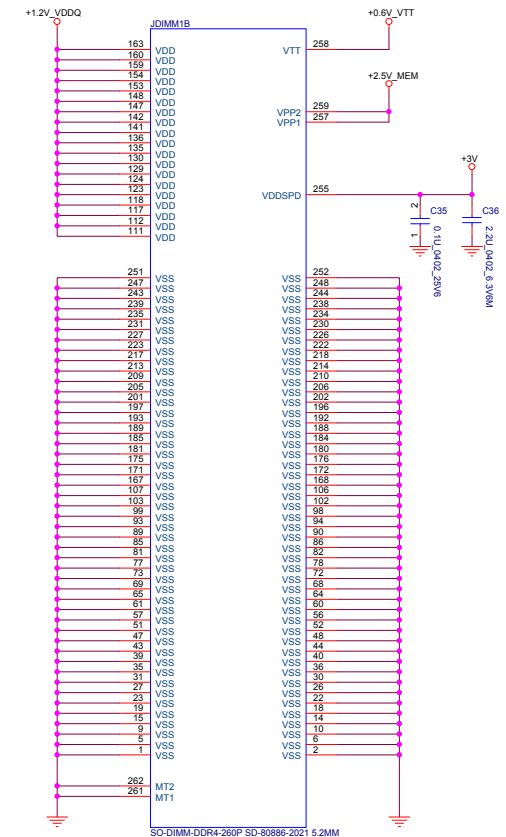
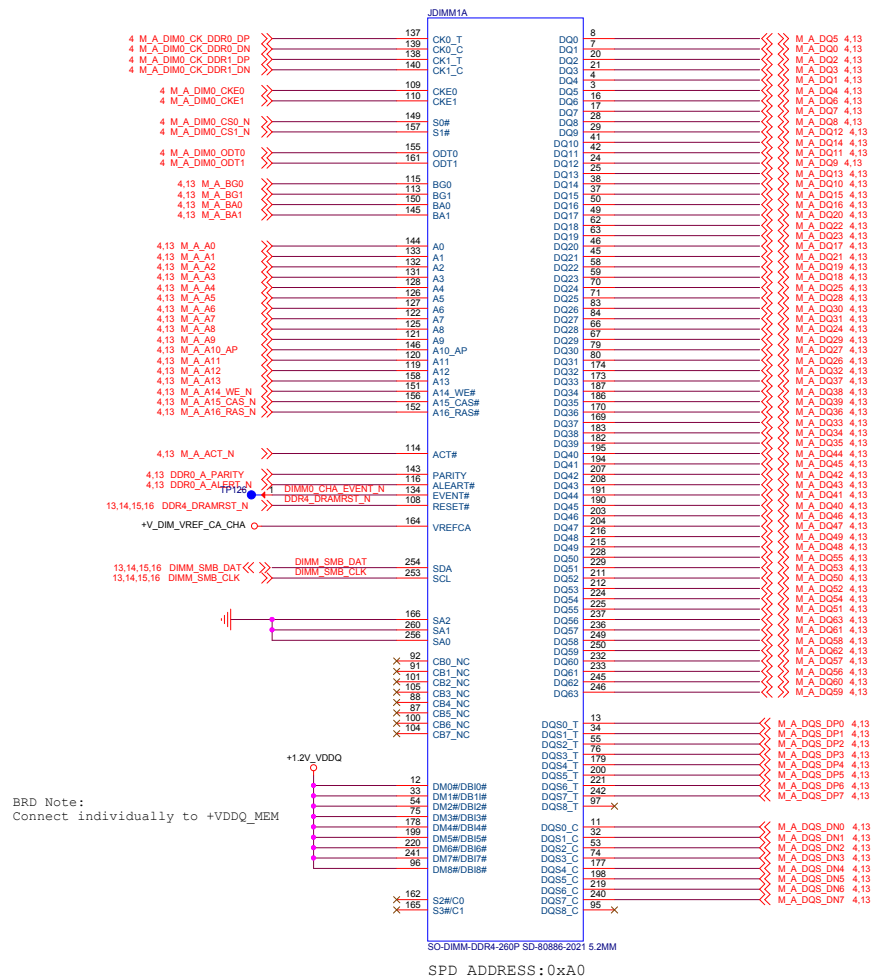
C1192 47U, 006K, 6.3V6K

C1193 47U, 006K, 6.3V6K

C1194 47U, 006K, 6.3V6K

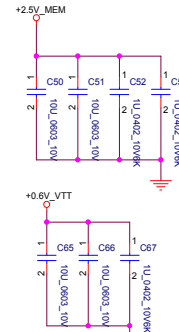
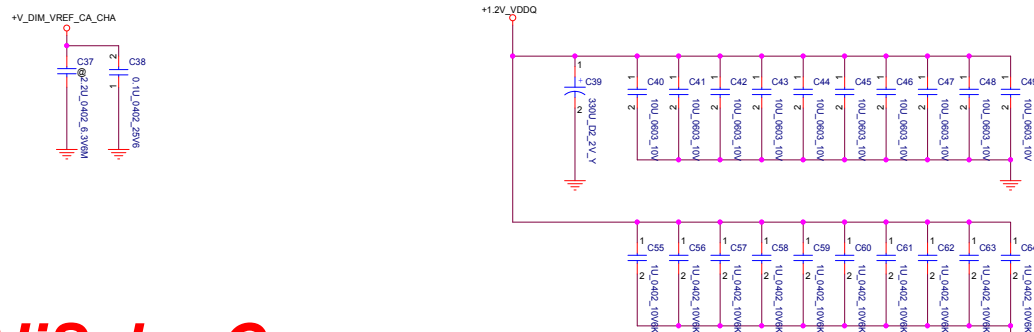
Date: Thursday, May 26, 2016 Sheet 11 of 99

DDR4 SODIMM CHANNEL - A BOTTOM REV DIMM0 (5.2 MM HEIGHT CONNECTOR)

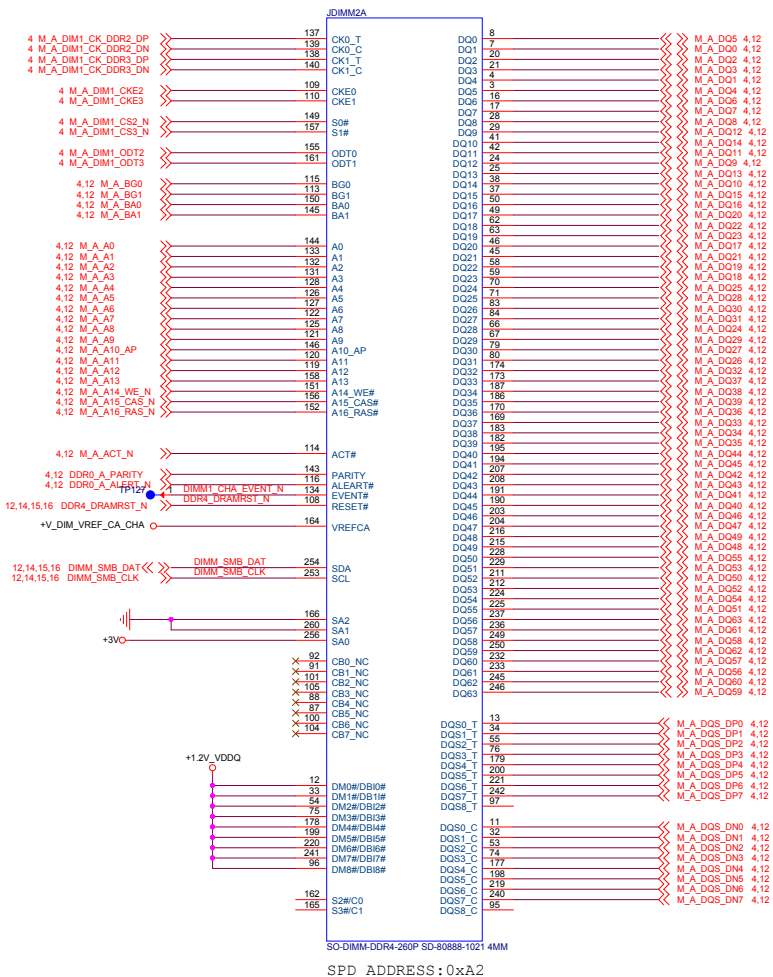


Decoupling Caps

BRD Note:
placed close to CHA DIMMO

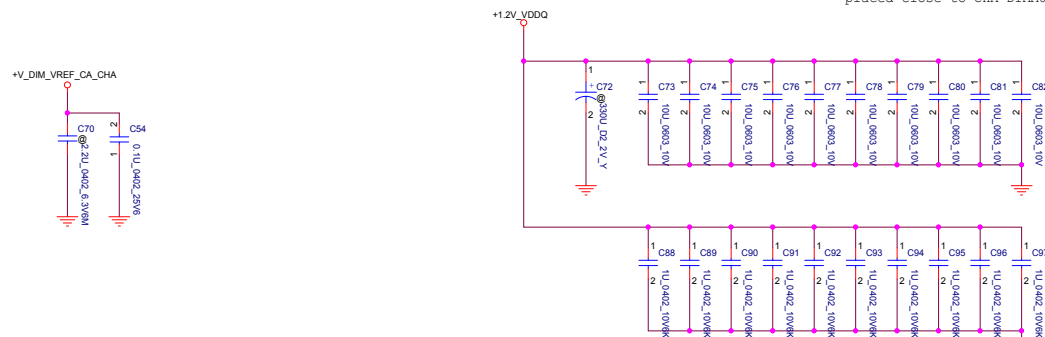


DDR4 SODIMM CHANNEL - A TOP STD DIMM1 (4 MM HEIGHT CONNECTOR)

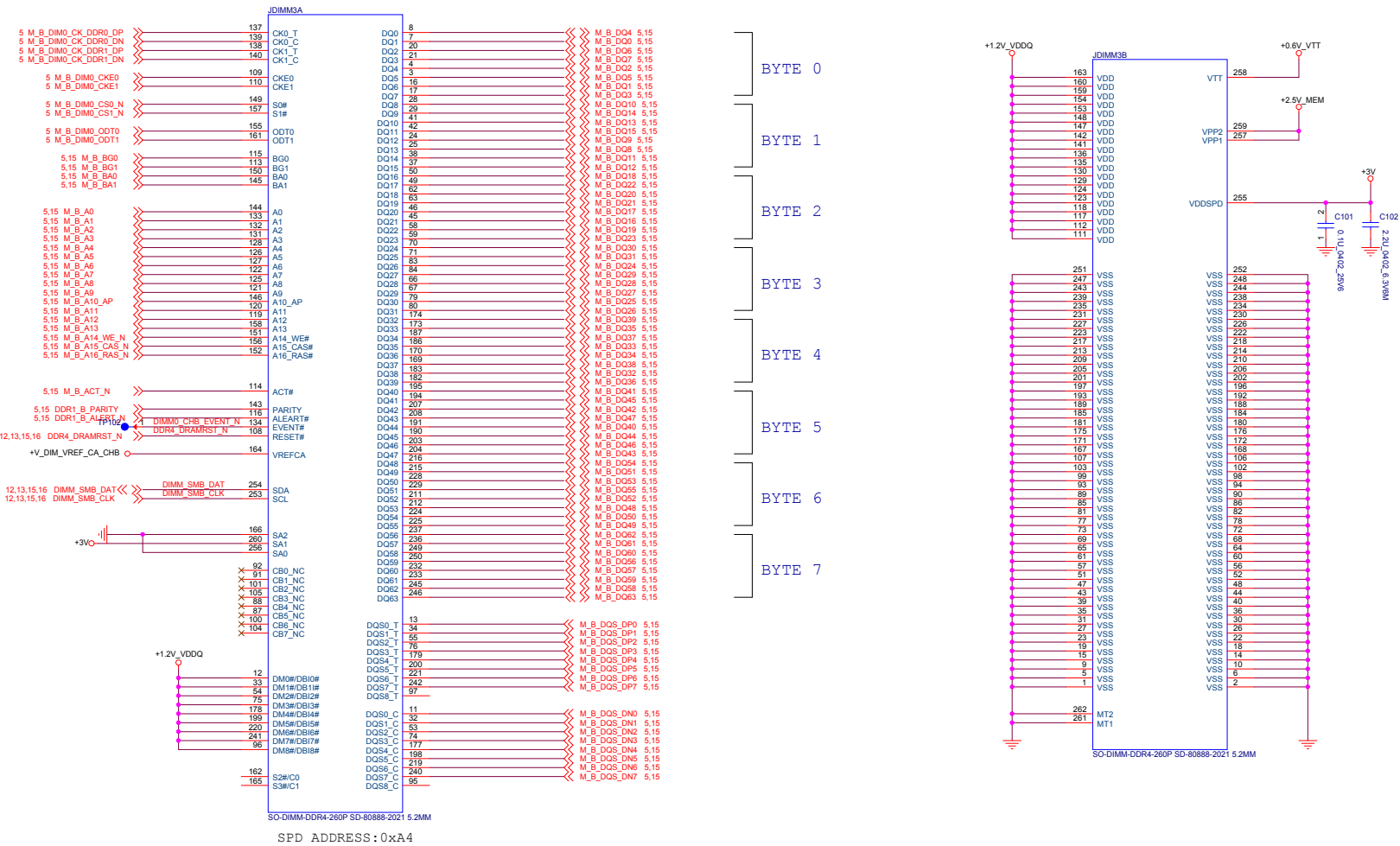


Decoupling Caps

BRD Note:
placed close to CHA DIMM0

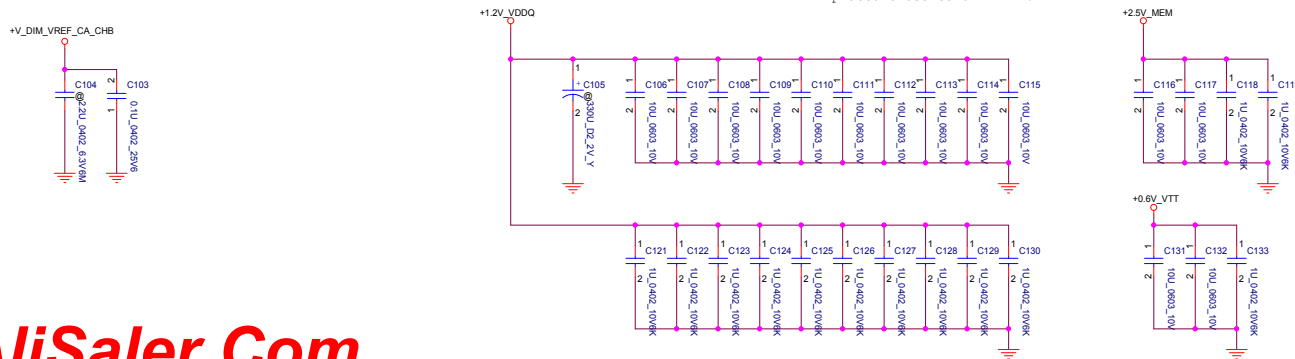


DDR4 SODIMM CHANNEL - B BOTTOM STD DIMM0 (5.2 MM HEIGHT CONNECTOR)



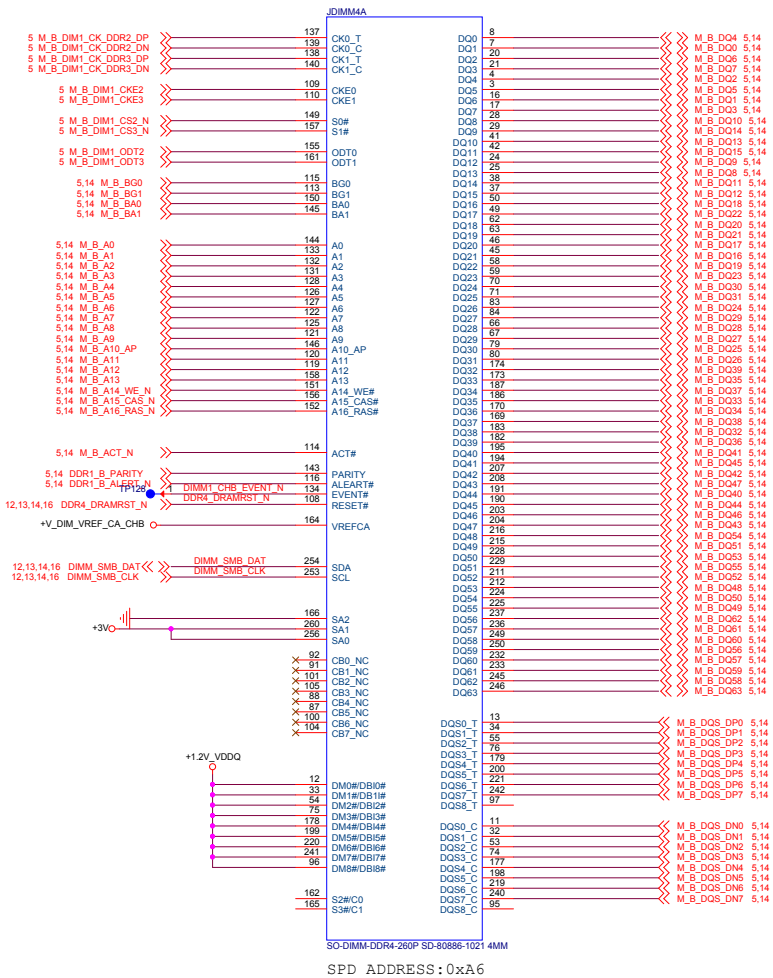
Decoupling Caps

BRD Note:
placed close to CHA DIMM0



lenovo 联想		LENOVO.CRDN	
File: DDR4 CHB DIMM0			
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DDR4 SODIMM CHANNEL - B TOP REV DIMM1 (4.0 MM HEIGHT CONNECTOR)



BYTE 0

BYTE 1

BYTE 2

BYTE 3

BYTE 4

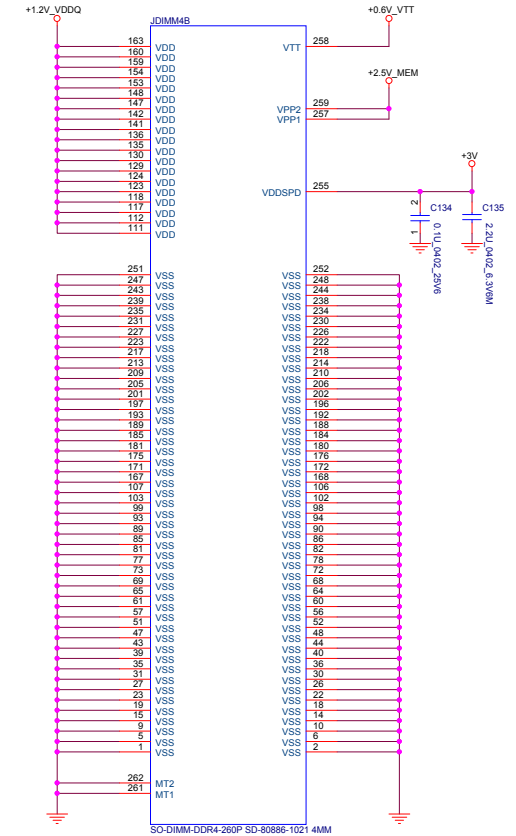
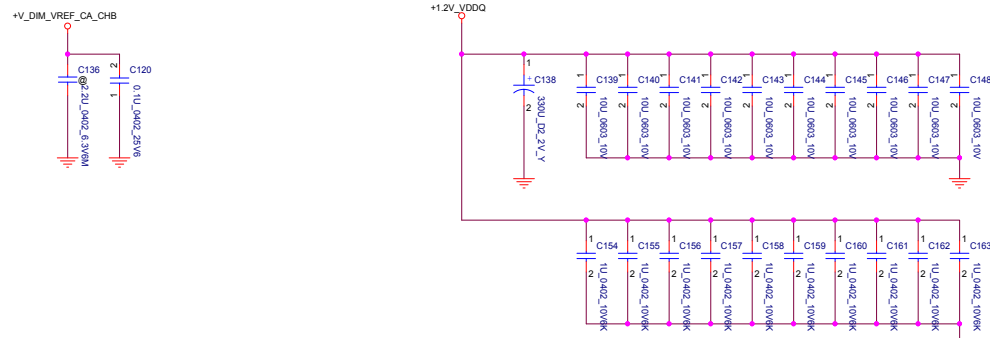
BYTE 5

BYTE 6

BYTE 7

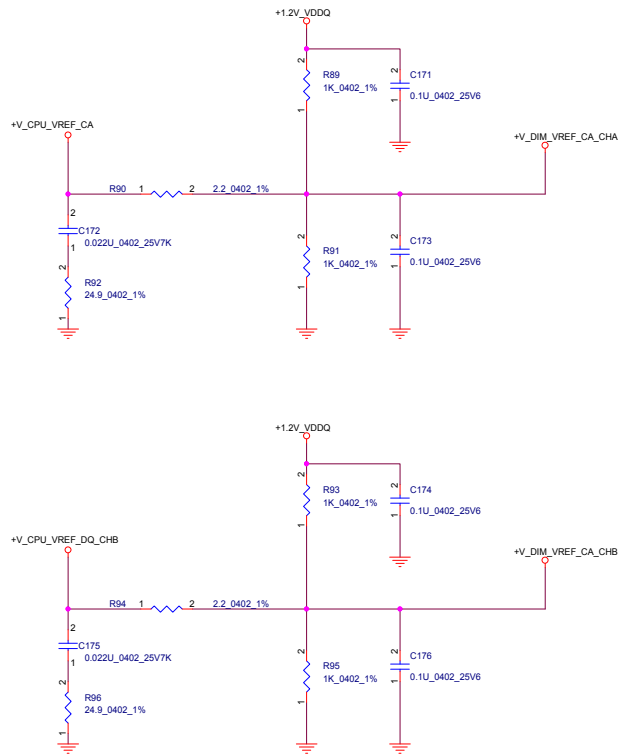
Decoupling Caps

BRD Note:
placed close to CHA DIMM0

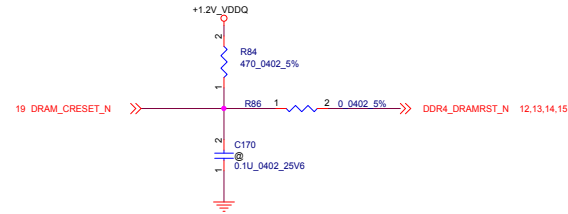


DDR VREF

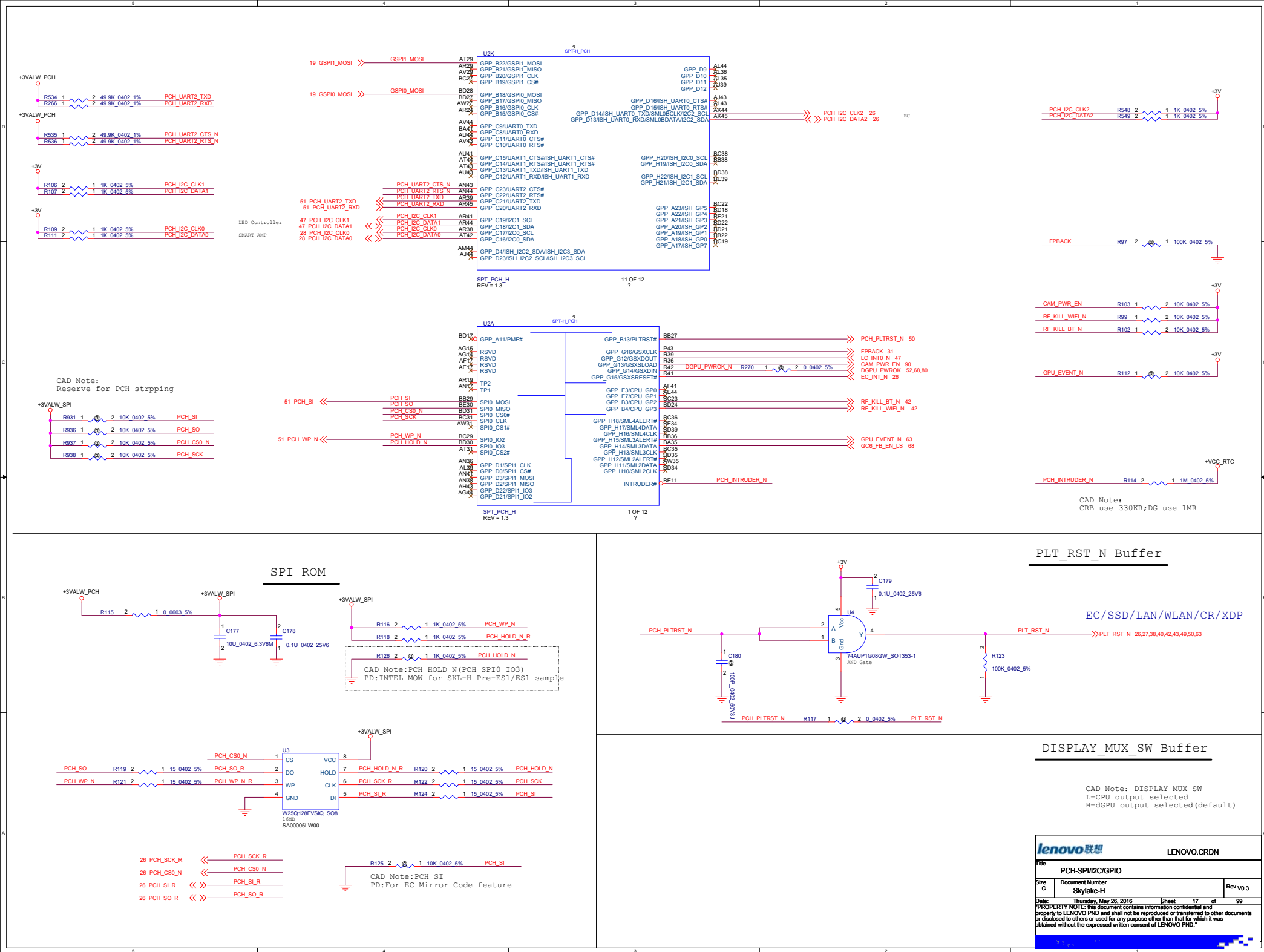
BRD Note:
VREF trace width 20mils;spacing 20 mils to other signal/planes



19.46.51 PCH_SMB_CLK << R81 1 2 0.0402 5% DIMM_SMB_CLK >>> DIMM_SMB_CLK 12,13,14,15
19.46.51 PCH_SMB_DAT << R82 1 2 0.0402 5% DIMM_SMB_DAT >>> DIMM_SMB_DAT 12,13,14,15



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File		DDR4-VREF	
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Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 7	USB3_7 / PCIE 1	AR (L0)	U2005 (Intel AR DP)	
Port 8	USB3_8 / PCIE 2	AR (L1)		
Port 9	USB3_9 / PCIE 3	AR (L2)		
Port 10	USB3_10 / PCIE 4	AR (L3)		
Port 11	PCIE 5	NC		
Port 12	PCIE 6	Card Reader	U3001	PCIE 1x Gen2
Port 13	PCIE 7	WLAN	JWLAN1	PCIE 1x Gen2
Port 14	PCIE 8	LAN	U6	PCIE1x Gen1

USB2.0 Configuration		
USB2 #	Assignment	OCx #
USB2 1	JUSB3(IO DB)	USB_OC0_N
USB2 2	JUSB2	USB_OC1_N
USB2 3	HD camera	
USB2 4	KB	
USB2 5	BT	
USB2 6	JUSB4(IO DB)	USB_OC3_N
USB2 7	NC	
USB2 8	NC	
USB2 9	NC	
USB2 10	NC	
USB2 11	NC	
USB2 12	NC	
USB2 13	NC	
USB2 14	NC	

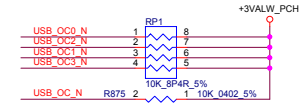
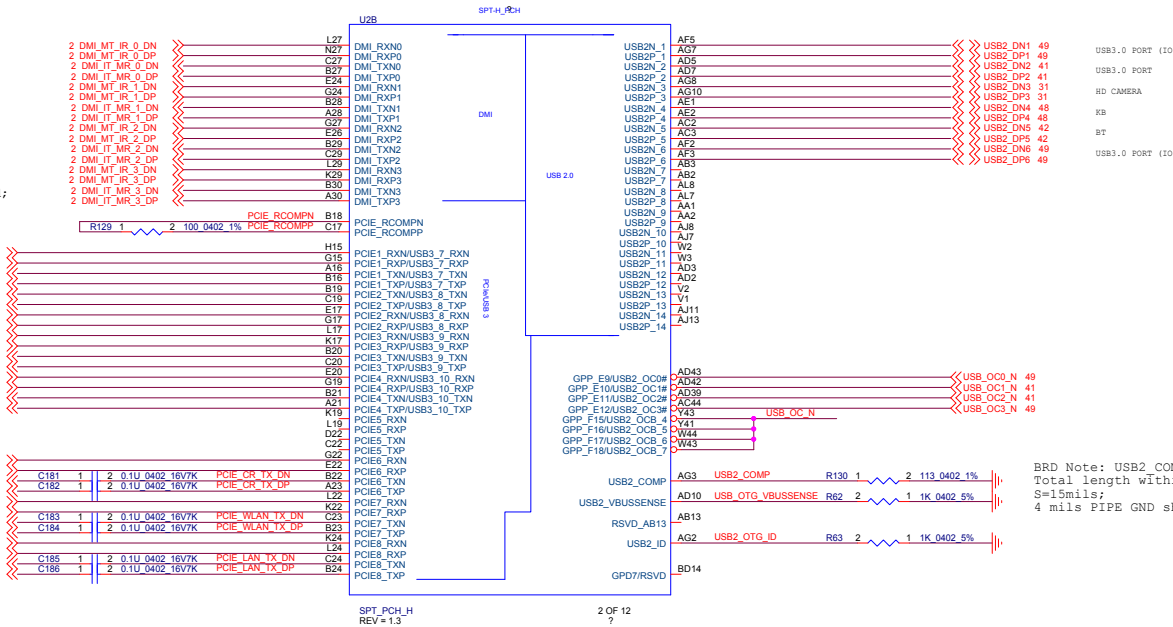
BRD Note: PCIE_RCOMP*
W=15mils;S=15mils;
4 mils PIPE GND shielding required;
Avoid routing next to clock
Length matched within 1%

Card Reader

WLAN

LAN

BRD Note: PCIE BUS
All the AC-coupling caps placed close to device down or connector;
Non-interleaved breakout is required



BRD Note: USB2_COMP
Total length within 1 inch;
S=15mils;
4 mils PIPE GND shielding suggested

lenovo 联想		LENOVO.CRDN	
File PCH-DM/PCIE/USB2.0			
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28 HDA_BCLK << R131 2 1 33 0402 5% HDA_BCLK_R
28 HDA_SYNC << R132 2 1 33 0402 5% HDA_SYNC_R
28 HDA_SDOUT << R134 2 1 33 0402 5% HDA_SDOUT_R
28 ME_FLASH << R2286 1 2 0 0402 5%

28 HDA_RST_N << R135 2 1 33 0402 5% HDA_RST_N_R
CAD Note: HDA_RST_N
Reserve and use the codec internal RST# default

R147 1 2 10K 0402 5% PM_PCH_PWROK
R149 1 2 10K 0402 5% PM_RSMRST_N
R547 1 2 10K 0402 5% PCH_GPP_B23

CAD Note: PCH_GPP_B23
Reserve for PCH stripping

+3VALW_PCH
R150 2 1 1K 0402 5% SML0_CLK
R151 2 1 1K 0402 5% SML0_DATA
R153 2 1 1K 0402 5% SMB_CLK
R155 2 1 1K 0402 5% SMB_DATA
R158 2 1 1K 0402 5% SML1_CLK
R159 2 1 1K 0402 5% SML1_DATA

HDA_BCLK_R BA9
HDA_RST# B08
HDA_SDO B07
HDA_SDI1 B06
HDA_SDO B09
HDA_SYNC B08
RSVD_B01 BD1
RSVD_BE2 BE2
DISPA_SDO AM1
DISPA_SDI AM2
DISPA_BCLK AL42
GPP_D8I2S0_SCLK AN42
GPP_D7I2S0_TXD AM43
GPP_D6I2S0_TXD AM43
GPP_D5I2S0_SFRM AH42
GPP_D2I2S0_DATA0 AJ35
GPP_D19I2S0_CLK0 AJ35
GPP_D18I2S0_CLK1 AJ35
GPP_D17I2S0_CLK1 AJ42
RTCRST_N BC10
SRTCST# BE10
PCH_PWROK AW11
RSMRST# BA11
DSW_PWROK BB41
SMB_CLK AW44
SMB_DATA BB43
SML0ALERT_N BA40
SML0_CLK BA40
SML0_DATA BB39
PCH_GPP_B23 AT27
SMLT_CLK AW42
SMLT_DATA AW45

U2D
SPT_H_PCH
GPP_A12I2S0_BUSY#ISH_GP6/SX_EXIT_HOLDOFF#
GPP_ABICLKRUN#
GPD11/LANPHYPC
GPD9/SLP_ILAN#
DRAM_RESET#
GPP_B2I2S0_VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE#
GPP_B11
SYS_PWROK
BC13
PCIE_WAKE_N
GPP_D7I2S0_A4
GPP_D7I2S0_A4
SLP_ILAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#SUSPWRODNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROC/PWRGD
ITP_PMODE
JTAGX
JTAG_TMS
AP1
JTAG_TDO
JTAG_TDI
JTAG_TCK

CAD Note: PCH_VRALERT_N
ICC max throttling indicator for the
PCH voltage regulators

PCH_CLKRUN_N R138 2 1 8.2K 0402 5%
+3VALW_PCH
SYS_RESET_N R143 1 2 10K 0402 5%
PCH_VRALERT_N R137 1 2 10K 0402 5%
PCH_VRALERT_N R138 1 2 10K 0402 5%
PM_BATLOW_N R139 2 1 8.2K 0402 5%
AC_PRESENT R142 1 2 10K 0402 5%
PCH_LAN_WAKE_N R288 1 2 10K 0402 5%
PCH_PWRBTN_N R381 2 1 100K 0402 5%
SYS_PWROK R146 1 2 10K 0402 5%
SUSCLK R148 1 2 10K 0402 5%

CAD Note: PCH_PWRBTN_N
PCH internal PU and Iems de-bounce

PCH Straps

+VCC_RTC
CAD Note:
CRB use 30.1KR;DG use 20KR
R160 2 1 20K 0402 1% SRTCST_N
C187 1 10 0402 10V6K
R163 2 1 20K 0402 1% RTCRST_N
C188 1 10 0402 10V6K
TP77
TP78

+3V
R164 2 1 1K 0402 5% HDA_SPKR

+3VALW_PCH
R167 2 1 1K 0402 5% HDA_SDOUT

+3V
R168 2 1 1K 0402 5% GSP10_MOSI 17

+3V
R169 1 2 4.7K 0402 5% SMBALERT_N

+3V
R170 2 1 1K 0402 5% SML0ALERT_N
R372 2 1 20K 0402 1%

+3V
R171 2 1 1K 0402 5% GSP11_MOSI 17
R506 2 1 20K 0402 1%

ME RESET

SRTCST_N 1:SAVE ME (Default) *
0:CLEAR ME

CMOS RESET

RTCRST_N 1:SAVE CMOS (Default) *
0:CLEAR CMOS

Top Swap MODE

HDA_SPKR 1:Enabled
0:Disabled(Default),Internal PD*

Flash Descriptor Security Override

HDA_SDOUT 1:Disabled
0:Enabled(Default),Internal PD *

TCO Timer System No Reboot mode

GSP10_MOSI 1:Enable "No reboot" mode
0:Disable (Default),Internal PD*

Intel ME TLS cipher suite

SMBALERT_N 1:Enabled
0:Disabled(Default),Internal PD*

eSPI or LPC bus for EC

SML0ALERT_N 1:eSPI
0:LPC(Default),Internal PD *

Boot BIOS Destination Bit 10

GSP11_MOSI 1:LPC
0:SPI(Default),Internal PD *

SMBus Isolation

+3V
R161 2 2.2K 0402 5%
R162 2 2.2K 0402 5%
SMB_CLK >>> PCH_SMB_CLK 16,46,51
SMB_DATA >>> PCH_SMB_DAT 16,46,51
Q1A AOS804EL_SC89-6
Q1B AOS804EL_SC89-6

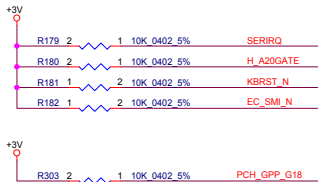
SODIMM/TP/XDP

+3V
R165 2 2.2K 0402 5%
R166 2 2.2K 0402 5%
SML1_CLK >>> EC_SMB_CLK1 26,45,63
SML1_DATA >>> EC_SMB_DAT1 26,45,63
Q2A AOS804EL_SC89-6
Q2B AOS804EL_SC89-6

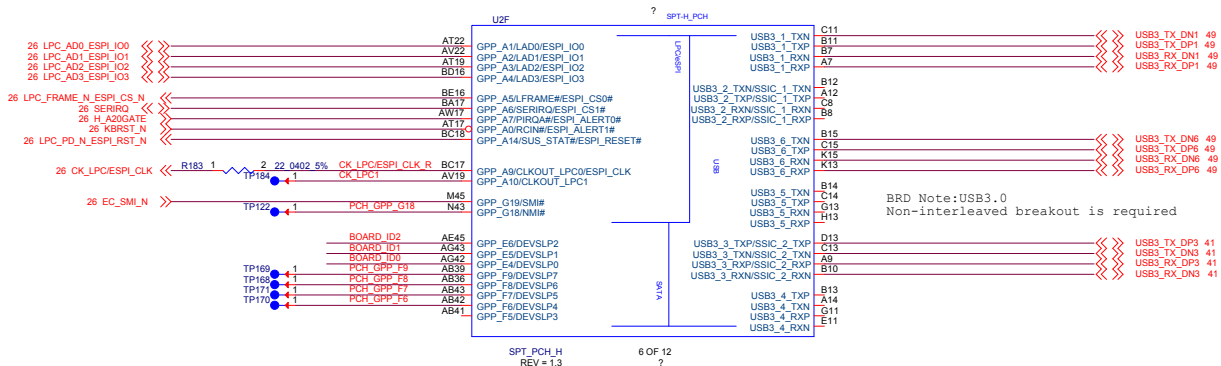
EC

EC Clear CMOS

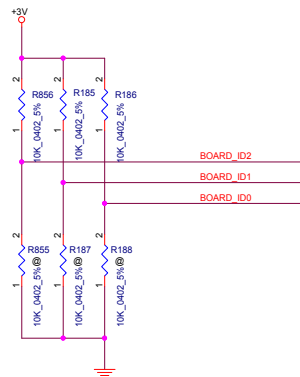
CAD Note: EC_CLEAR_CMOS
LOW:Keep CMOS
Hi:Clear CMOS
26 EC_CLEAR_CMOS >>> EC_CLEAR_CMOS
R428 1 20K 0402 1%
C401 1 10 0402 10V6K
Q12 DMG1012T-7_SOT523-3
RTCRST_N



CAD Note:
LPC:24M Hz
eSPI:20/30/60M Hz



Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	OCx #
Port 1	USB3 1 Capable of OTG	USB3.0	JUSB3(IO DB)	USB_OC0_N
Port 2	USB2 3 / SSIC 1	NC		
Port 3	USB3 3 / SSIC 2	USB3.0	JUSB2	USB_OC1_N
Port 4	USB3 4	NC		
Port 5	USB3 5	NC		
Port 6	USB3 6	USB3.0	JUSB4(IO DB)	USB_OC3_N



BOARD_ID2	BOARD_ID1	BOARD_ID0	Description
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

File

PCH-USB3.0/LPC

Size

C

Document Number

Skylake-H

Date

Thursday, May 26, 2016

Sheet

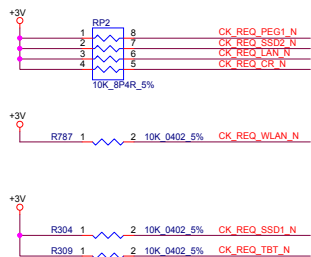
21

of

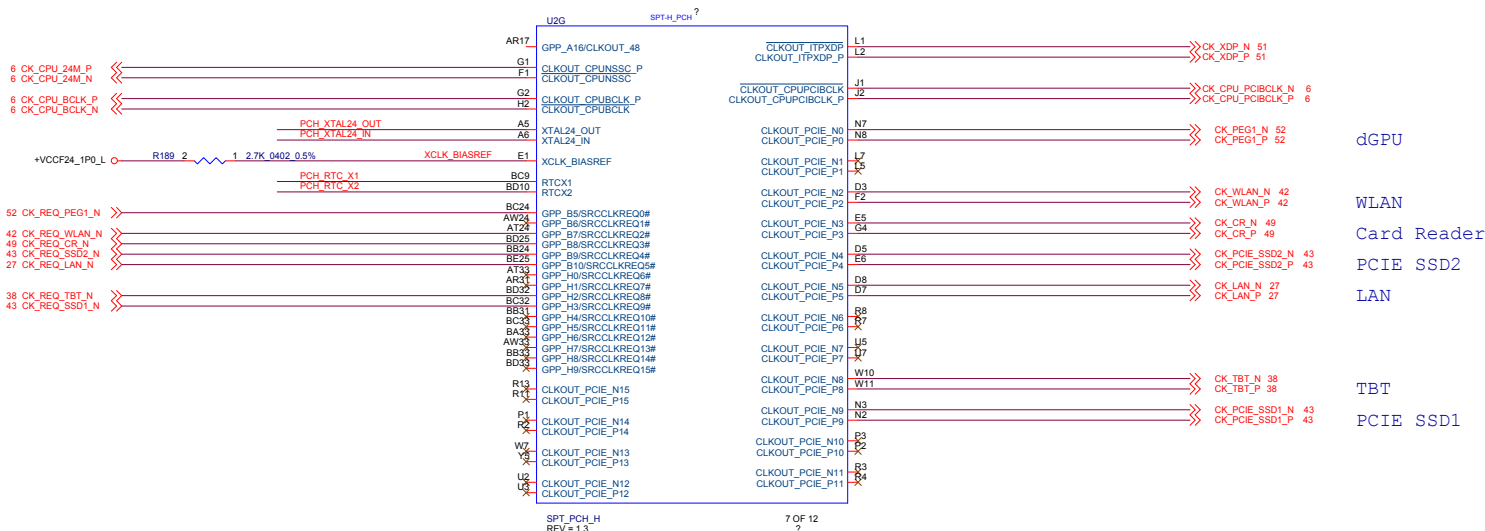
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PROPERTY NOTE:

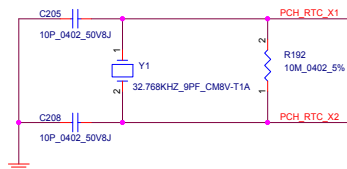
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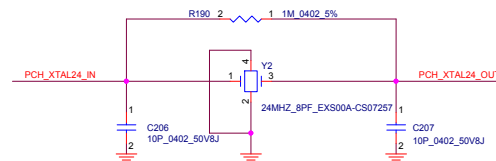
BRD Note: XCLK_BIASREF
Ground reference;Max via:2
Isolation spacing:20mils
Segment Length:100mils;Total length:1000mils
VSS shield recommended;S:W:S=6:4:6



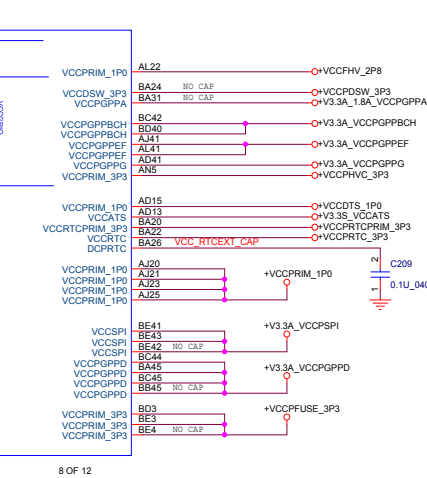
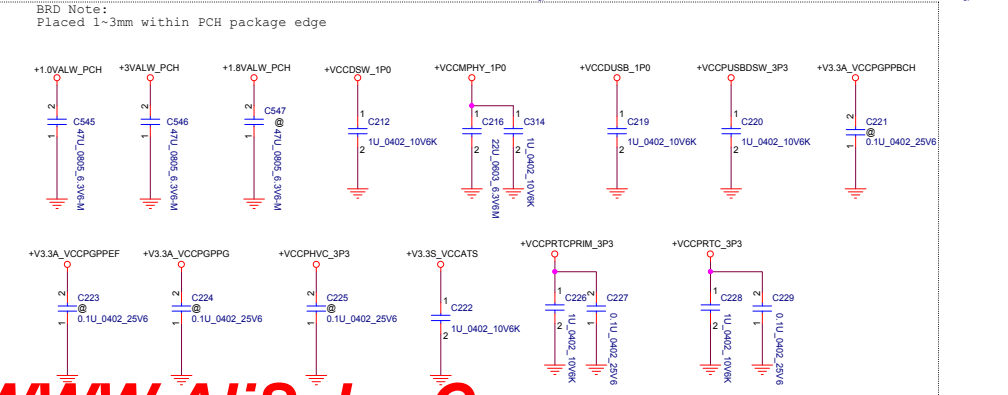
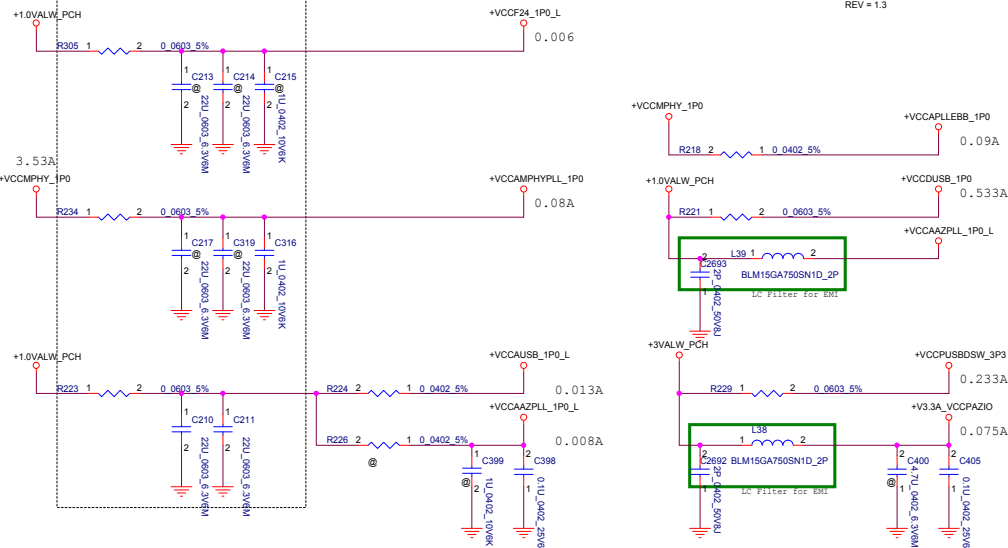
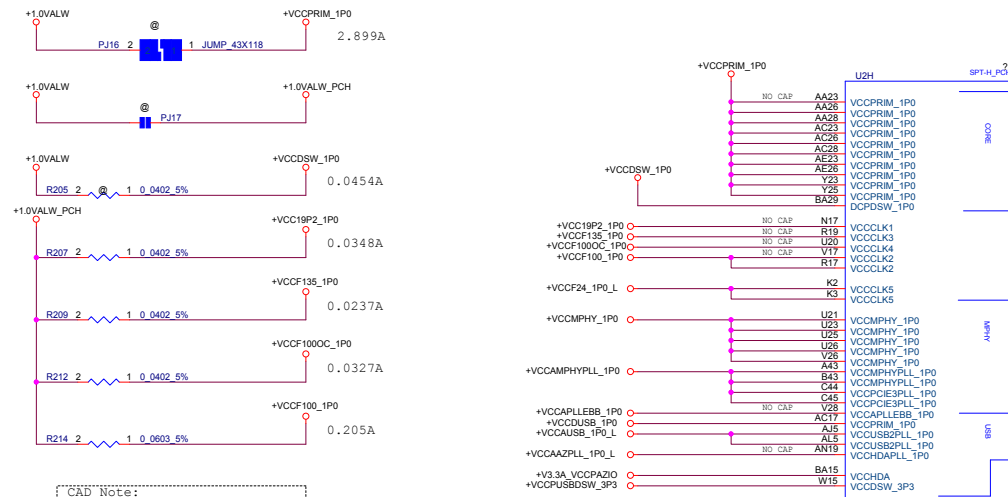
CAD Note:
Max crystal ESR 50K ohm



BRD Note:
Z0=50 ohm +/-15%;Ground reference;Max via:2
Group spacing:15mils;Isolation spacing:20mils
Segment Length:100mils;Total length:1000mils;Length match:100mils
VSS shield recommended;S:W:S=6:4:6

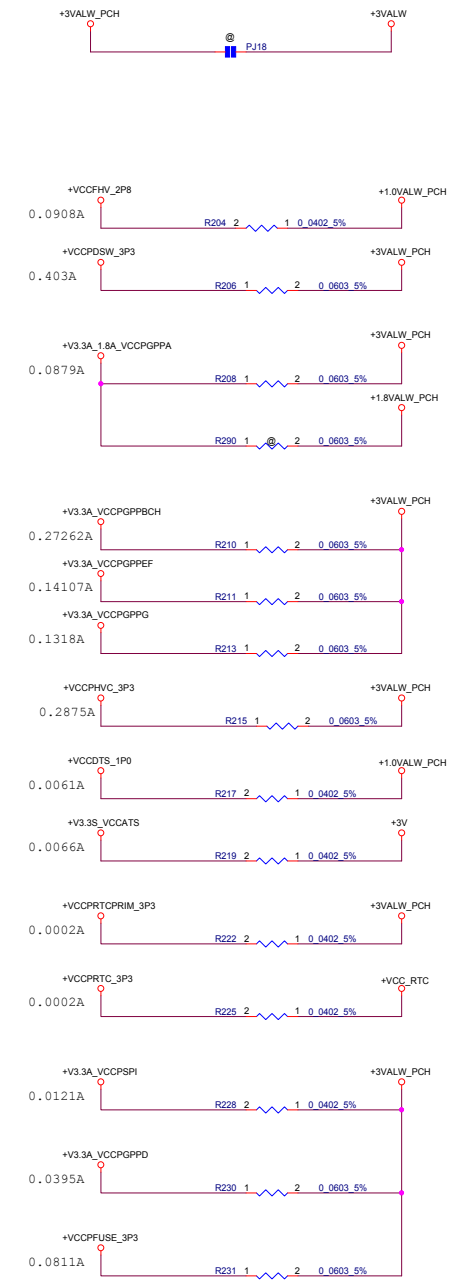


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File PCH-CLOCK			
Size C	Document Number	Rev V0.3	
Date: Thursday, May 26, 2016		Sheet 22 of 99	
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PCH POWER RAIL TABLE

POWER RAIL	LEVEL (v)	IccMAX current (A)	EDS
+VCCPRIM_1P0	1.0	2.899	
+VCC19P2_1P0	1.0	0.021	
+VCCF100_1P0	1.0	0.138	
+VCCF135_1P0	1.0	0.051	
+VCCF100OC_1P0	1.0	0.024	
+VCCMPHY_1P0	1.0	3.53	
+VCCAAZPLL_1P0_L	1.0	0.008	
+VCCAMPHYPLL_1P0	1.0	0.08	
+VCCAUSB_1P0_L	1.0	0.013	
+V3.3A_VCCPGPPA	3.3	0.084	
+V3.3A_VCCPGPPBCH	3.3	0.259	
+V3.3A_VCCPGPPD	3.3	0.101	
+V3.3A_VCCPGPPEF	3.3	0.134	
+V3.3A_VCCPGPPG	3.3	0.125	
+V3.3A_VCCPSPI	3.3	0.012	
+V3.3S_VCCATS	3.3	0.007	
+V3.3A_V1.8A_VCCPAZ	3.3	0.06	
+VCCPFUSE_3P3	3.3	0.3	
+VCCPUSBD SW_3P3	3.3	0.233	
+VCCPRTCPRIM_3P3	3.3	0.001	
+VCCPRTC_3P3	3.3	0.001	



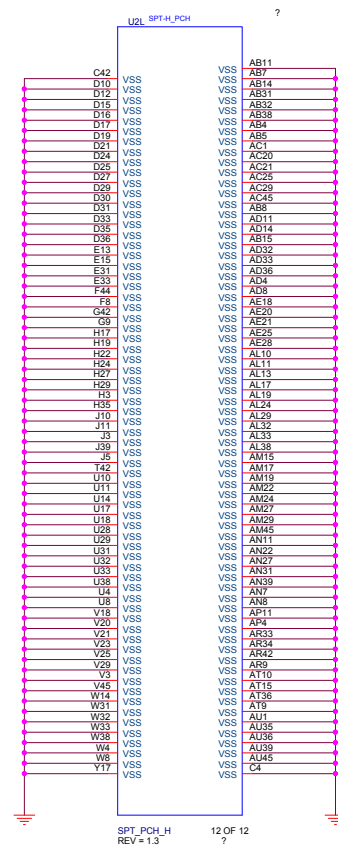
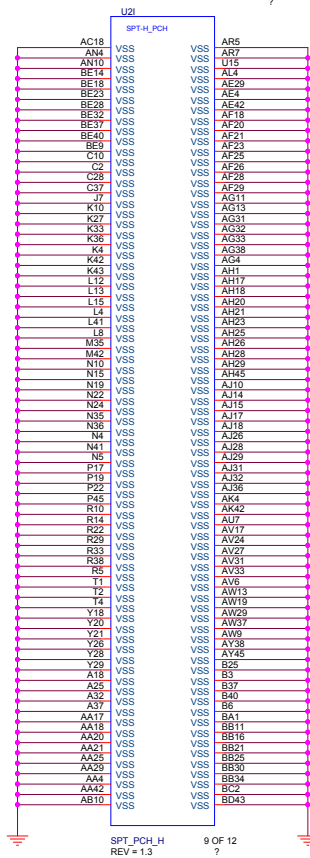
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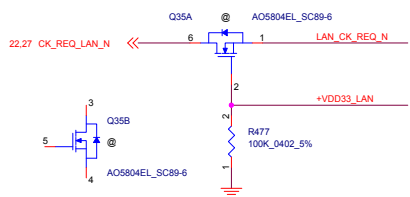
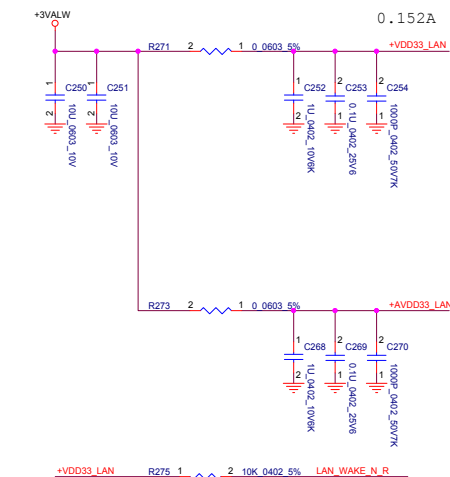
File PCH-POWER

Size C Document Number Skylake-H Rev v0.3

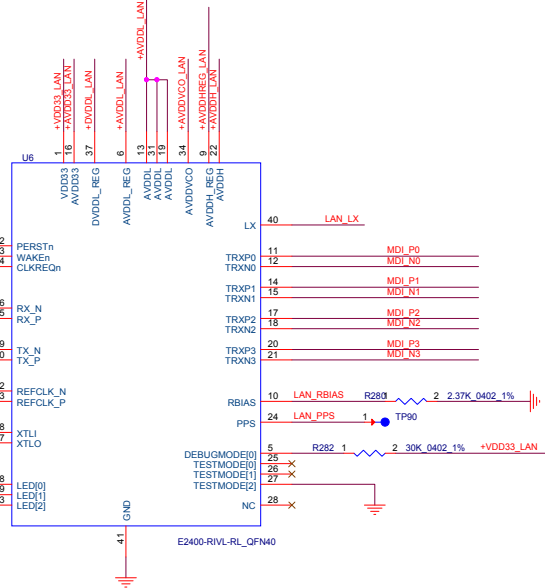
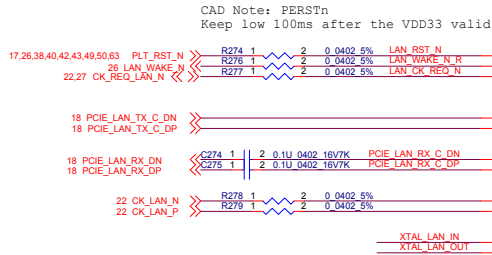
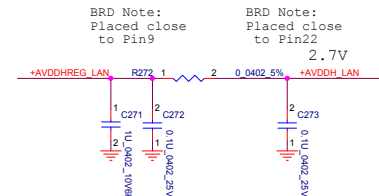
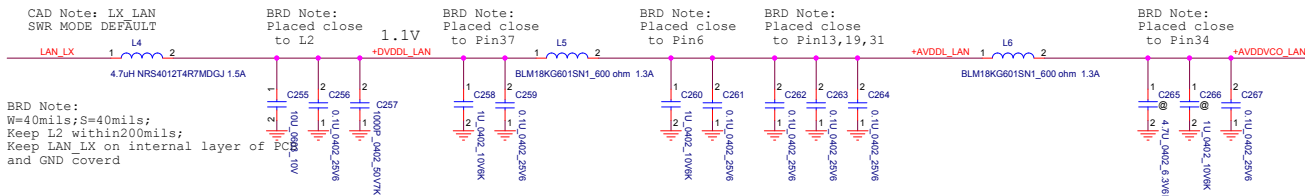
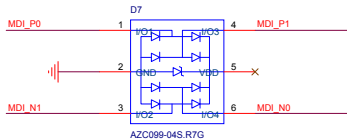
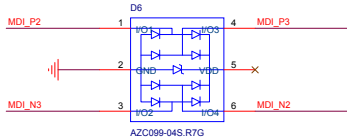
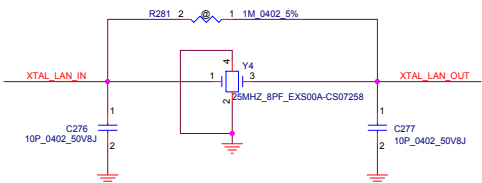
Date: Thursday, May 26, 2016 Sheet 24 of 99

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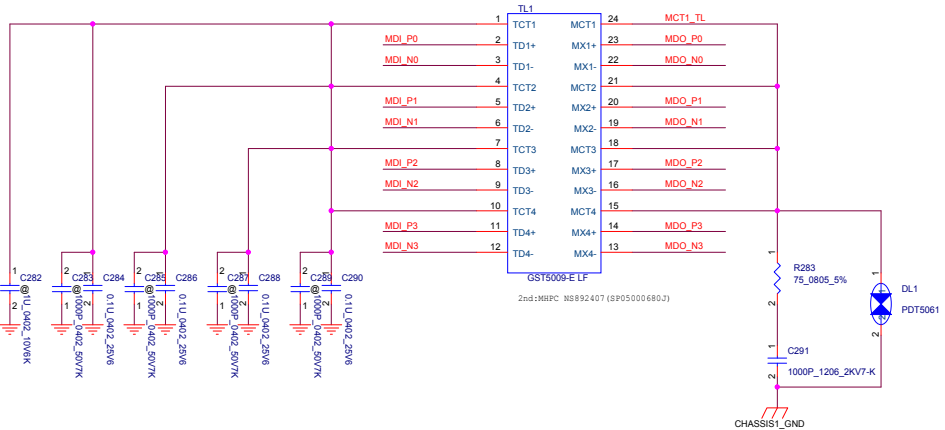
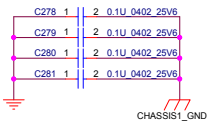
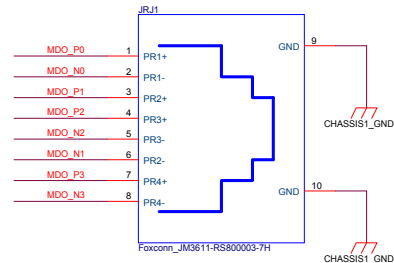
CAD Note: PECLK
Clock must be valid within 3ms
after the VDD33 reach 2.0V level



BRD Note: MDI*
Trace length between E-2011B and Transformer
be 1.5-10inch

BRD Note: LAN RBIAS
Keep away from other signals 25mils;
placed on the other side is possible

CAD Note: PPS
1 Hz clock output for IEEE1588 timing sync



BRD Note:
placed near to Pin6&7
and Pin41&42&43 separately

separate to two group and place need
C Pin6&7 and Pin42&43;

BRD Note:
Route 40 mils width and As short as possible

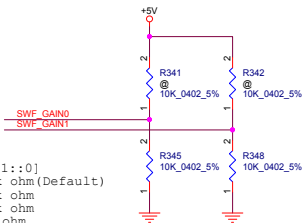
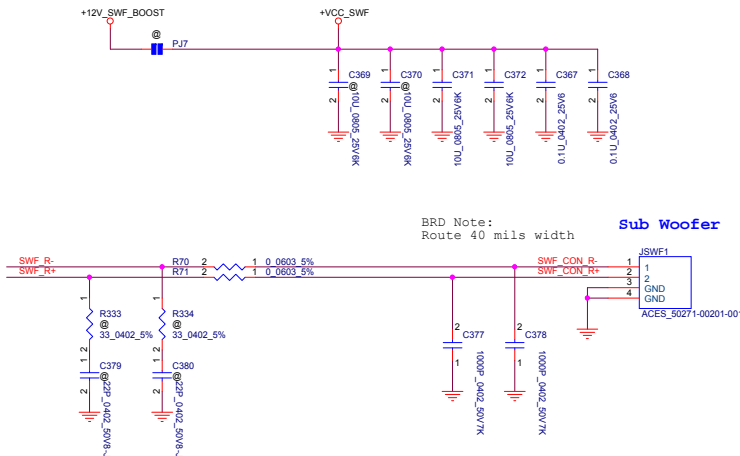
Internal Speaker


CAD Note: AMP PD R_N
Low active to mute,
Tr/Tf less than 20ns

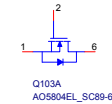
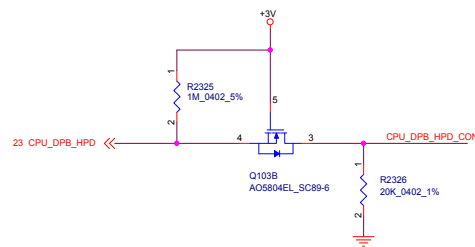
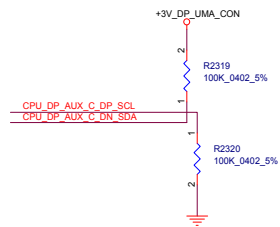
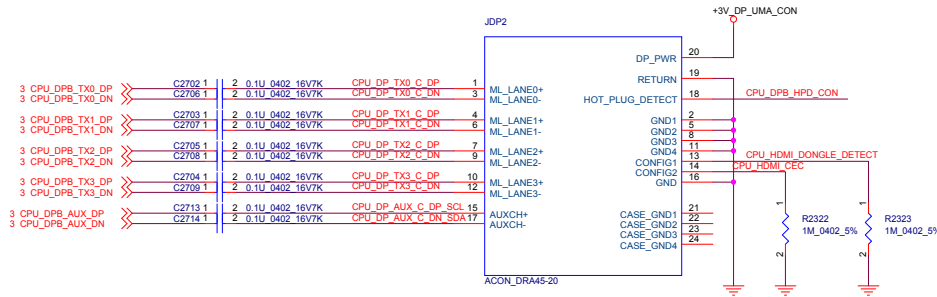
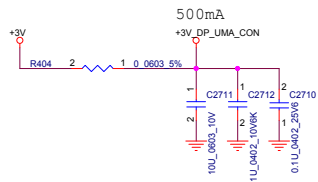
AMP_SPK_R+ R66 2 1 0.0603_5%
AMP_SPK_R- R67 2 1 0.0603_5%
AMP_SPK_L+ R68 2 1 0.0603_5%
AMP_SPK_L- R69 2 1 0.0603_5%

SPK_CON_R+
SPK_CON_R-
SPK_CON_L+
SPK_CON_L-

ACES_50281-00401-001

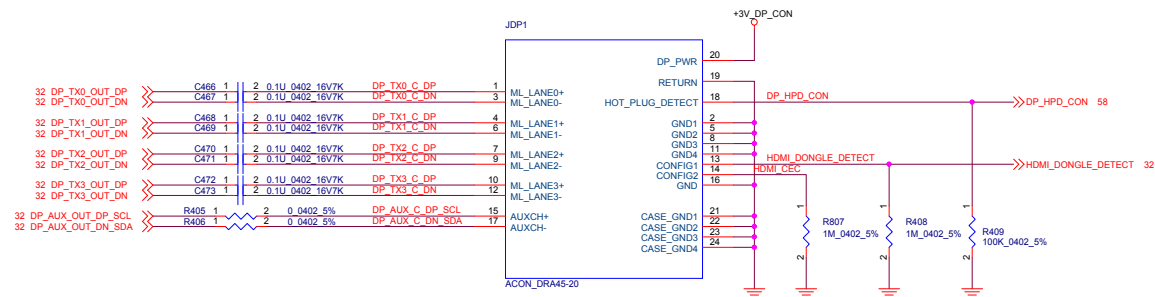


		LENOVO.CRDN	
Title AMP			
Size C	Document Number SkyLake-H		Rev V0.3
Date: Thursday, May 26, 2016	Sheet 29	of 99	
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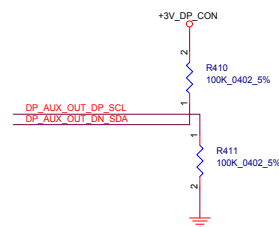




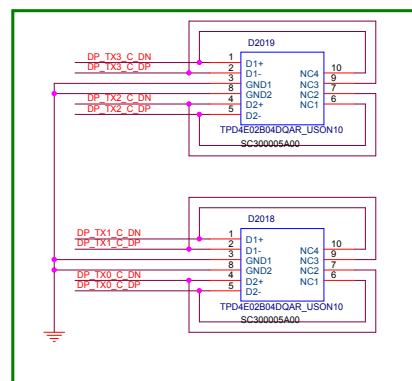




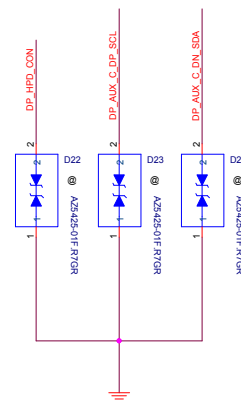
CAD Note: HDMI DONGLE DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED

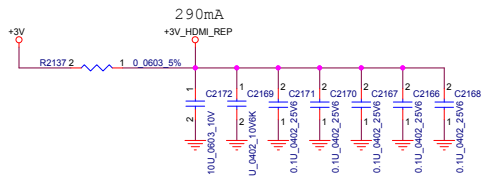


CAD Note: Reserve for ESD

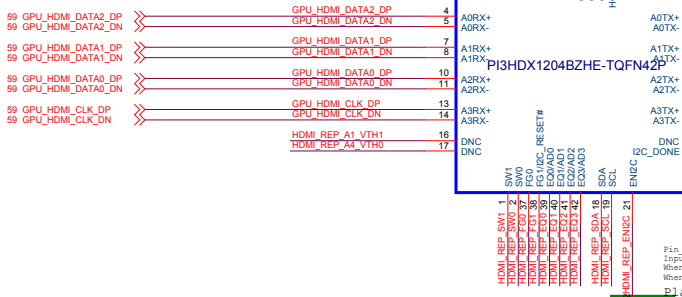


CAD Note: Reserve for ESD





AC coupling cap @ GPU side, and place close to U2019.



Pin Mode: (PI3HDX1204BZHE)
Input with internal 100k-Ohm Pull-Up.
When HIGH, each channel is programmed by the external pin voltage.
When LOW, each channel is programmed by the data stored in the I2C bus.
Place BOT side.

CAD Note:
Internal pull up at ~100kΩ, 3.3V I/O.

DE[1:0]=01, De-emphasis=3.5db
Inputs with internal 100k-Ohm Pull-Up.
This pins set the output De-emphasis Level in all channel when Pin_Mode is HIGH.

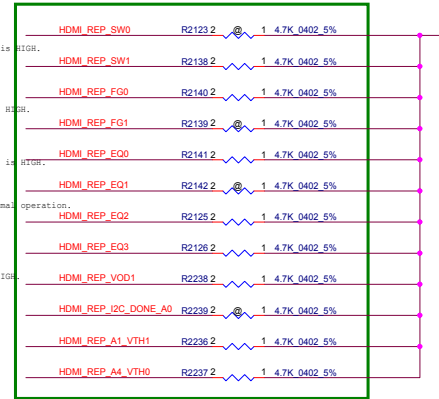
PS[1:0]=10, Pre-shoot=3.5db
Inputs with internal 100k-Ohm Pull-Up.
This pins set the output Pre-shoot Level in all channel when Pin_Mode is HIGH.

BST[3:0]:
Inputs with internal 100k-Ohm Pull-Up.
This pins set the amount of Equalizer Boost in all channel when Pin mode is HIGH.

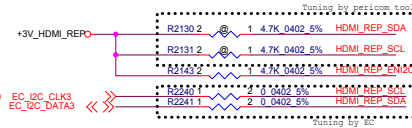
FEH: (PI3HDX1204B)
Power Enable with internal 100k-Ohm Pull-Up device is enabled and in normal operation.
Reserve 4.7K PD for PI3HDX1204D.

HDMI_REP_VDD1:
Inputs with internal 100k-Ohm Pull-Up.
This pin sets the output Voltage Level in all channel when Pin mode is HIGH.

A4/A1/A0:
I2C programmable address bits, with internal 100k-Ohm Pull-Up.
I2C Address=0xC2

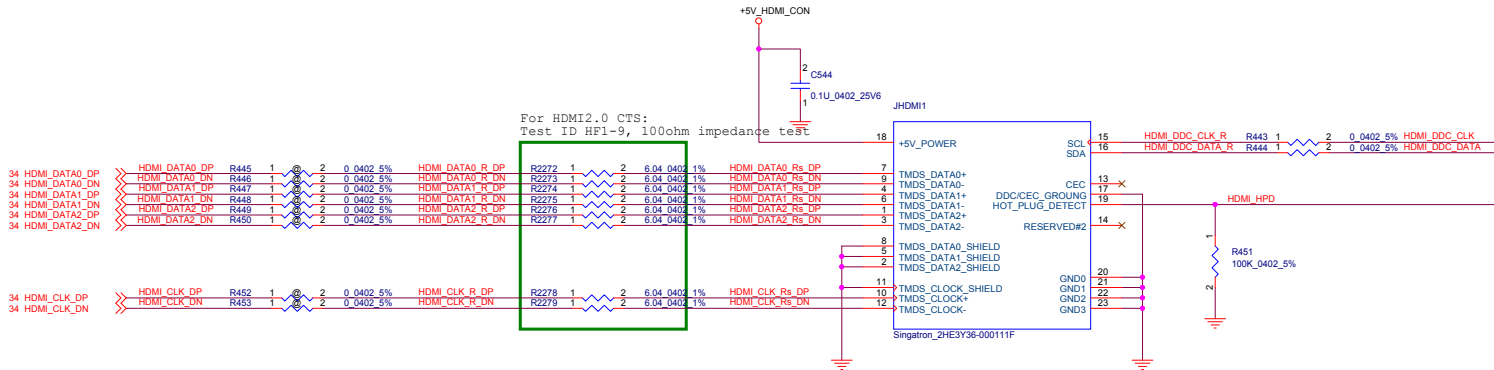


Place BOT side.



Place BOT side.

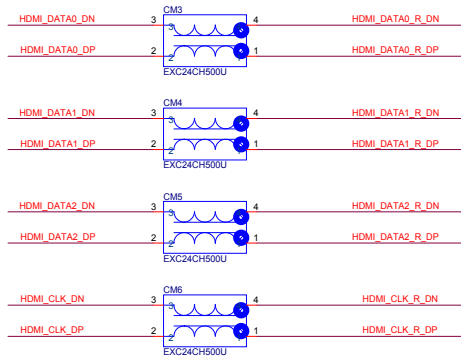
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Title: HDMI2.0 REPEATER			
Size: C	Document Number: SkyLake-H	Rev v0.3	
Date: Thursday, May 26, 2016	Sheet: 34	of 89	
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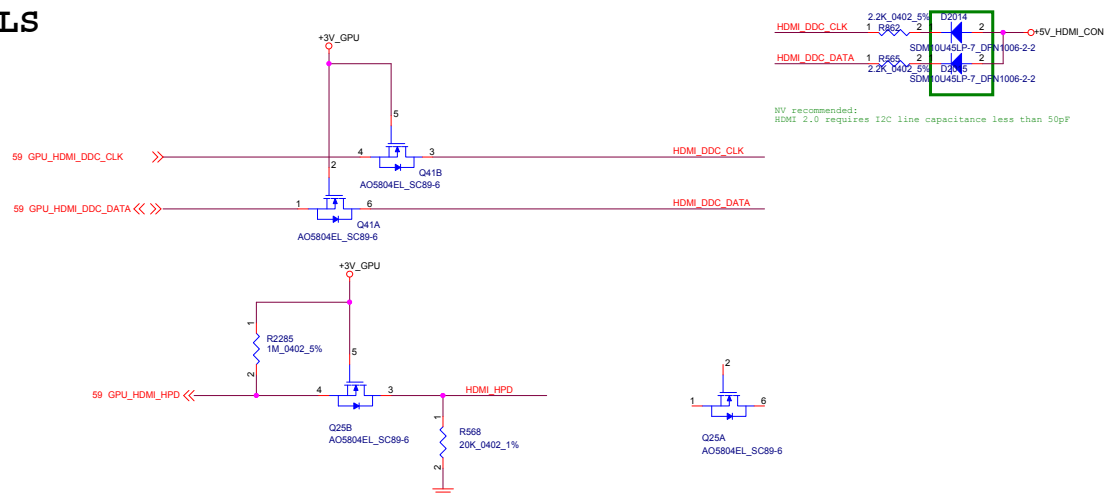
CM

BRD Note:
Co-lay with R

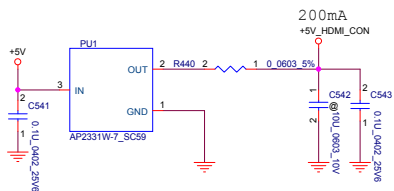
CAD Note:
Reserve for EMI



LS

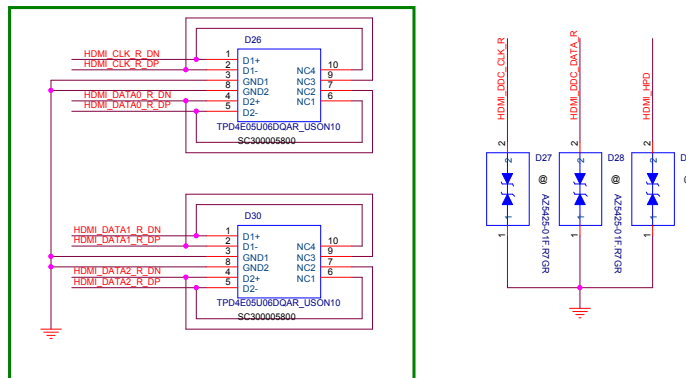


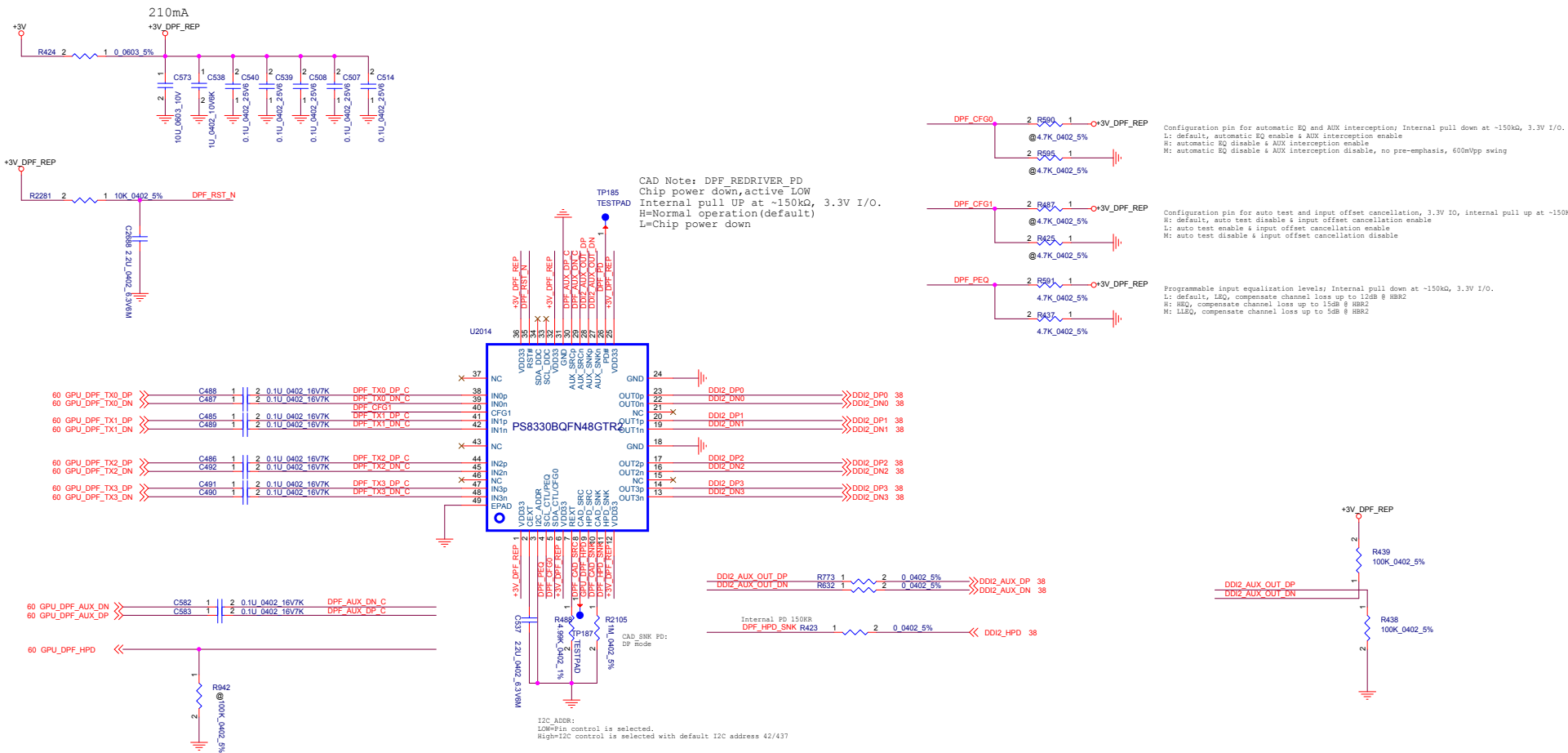
Power switch



ESD

CAD Note: Reserve for ESD





Automatic Power Down

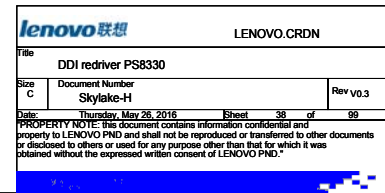


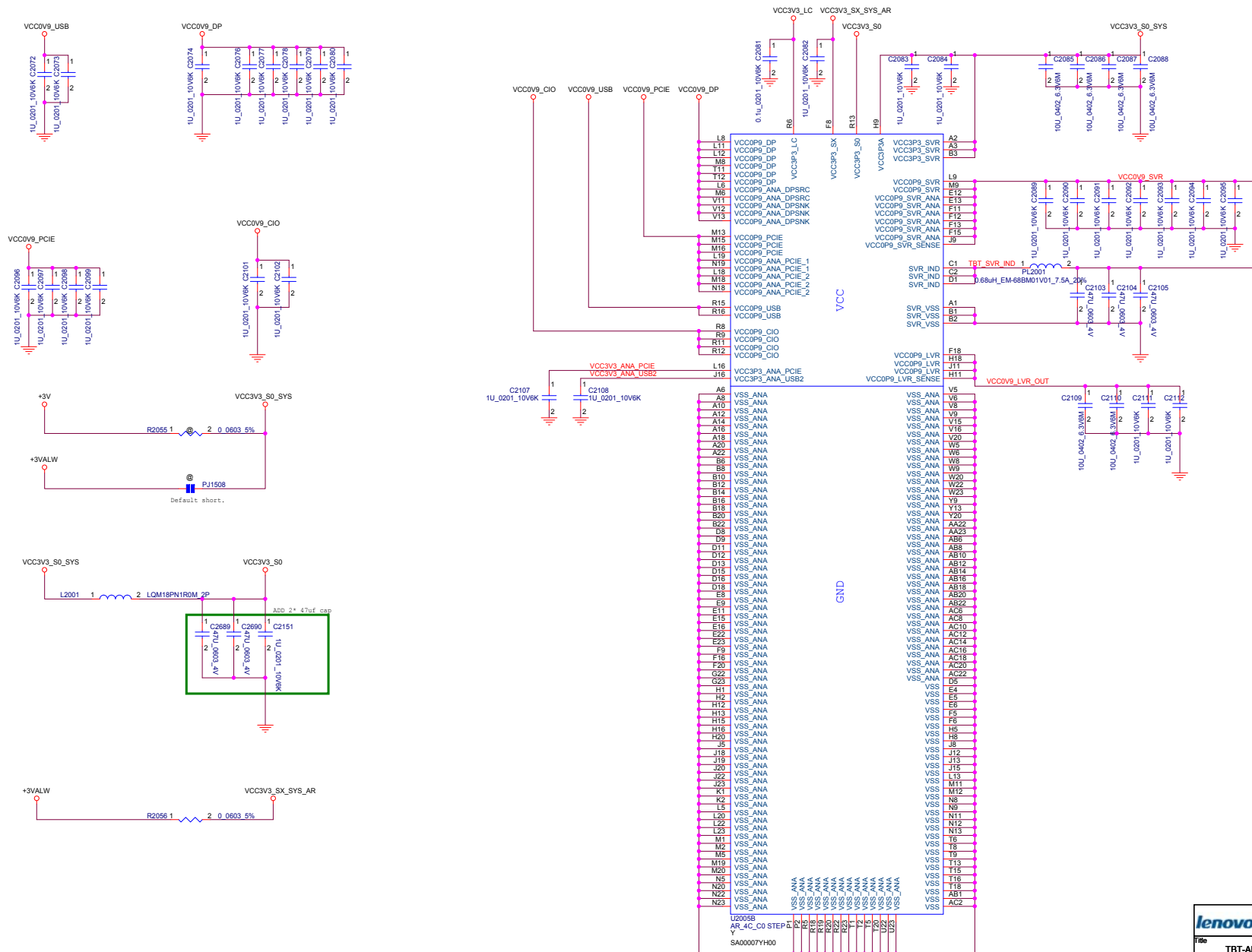
Figure 10. Automatic Power Down Timing

Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Timing (Figures 10)					
t1 _{HPD}	Propagation delay of HPD_SNK assertion at Power Down Mode to HPD_SRC assertion	100		400	ms
t3 _{HPD}	HPD pulse duration when treated as an IRQ			2	ms
t4 _{HPD}	Power down delay from HPD_SNK de-assertion to chip power down	400		1500	ms

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Title			
AR DP MUX-2			
Size		Document Number	Rev V0.3
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ROM





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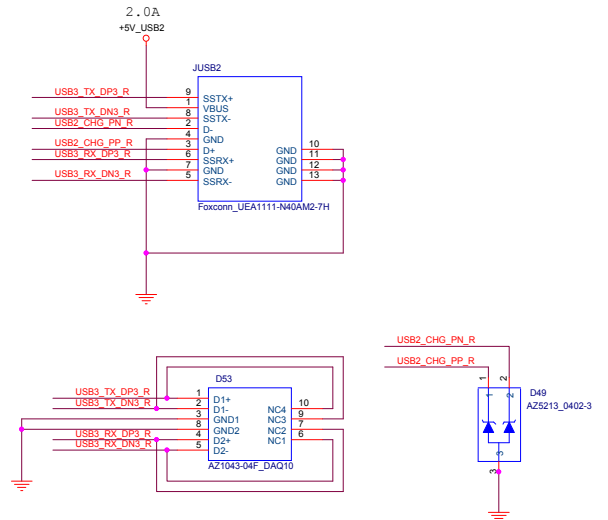
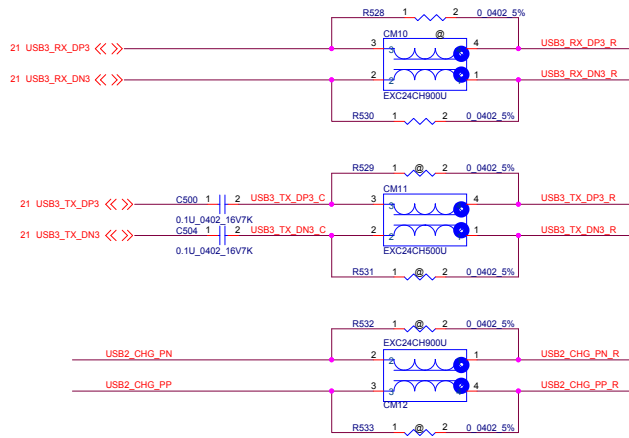
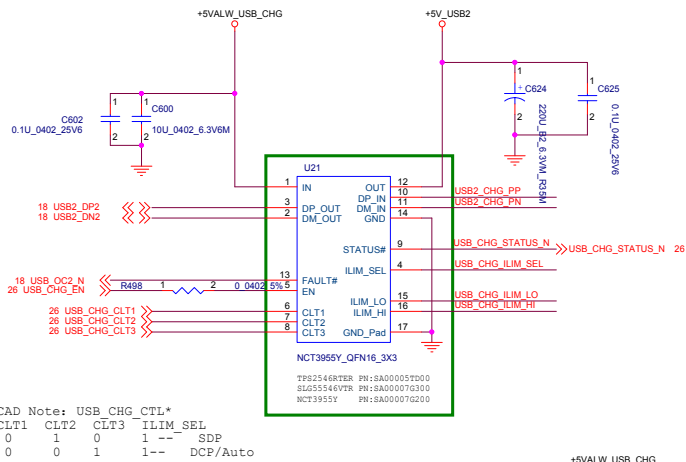
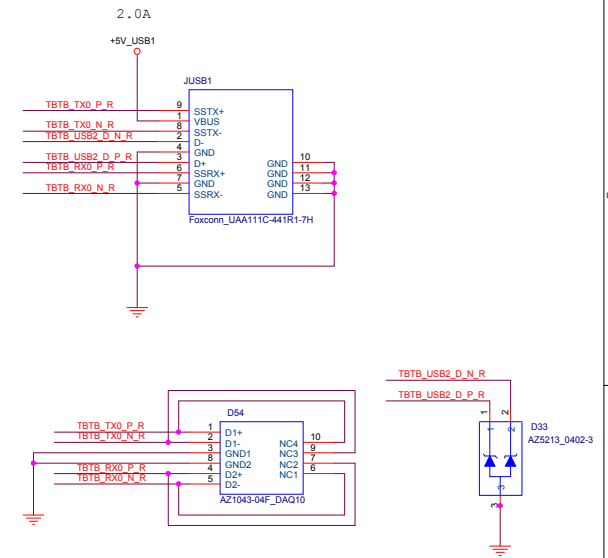
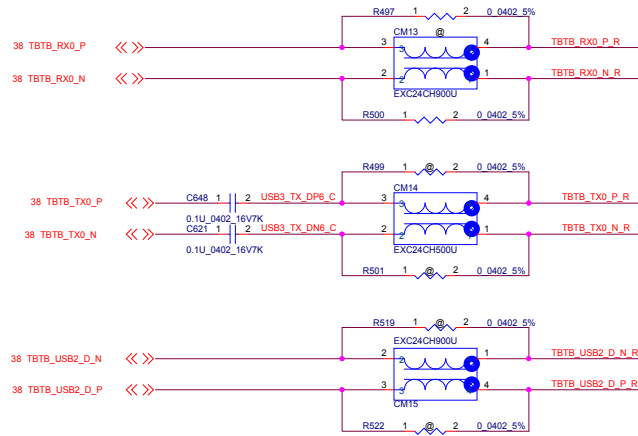
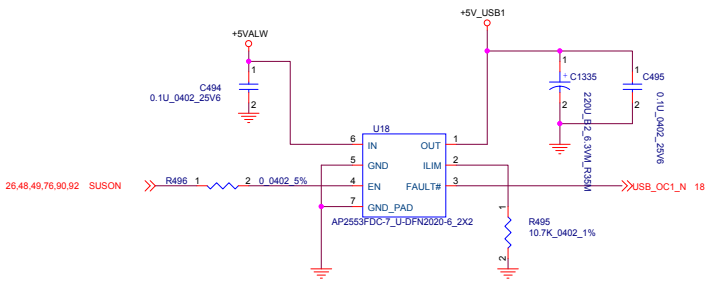
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TBT-AR POWER

Size C Document Number Skylake-H

Rev v0.3

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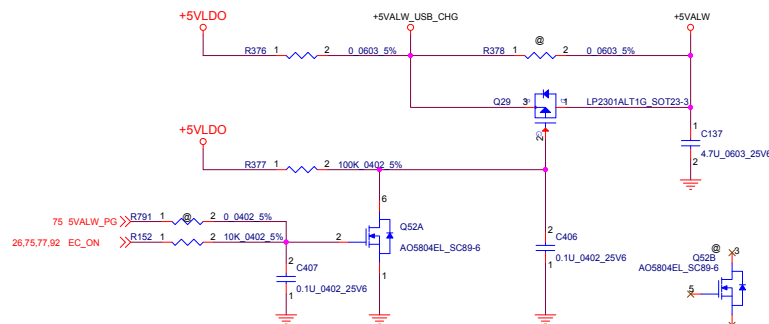


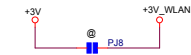
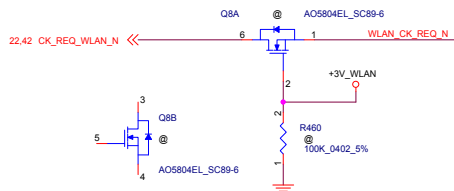
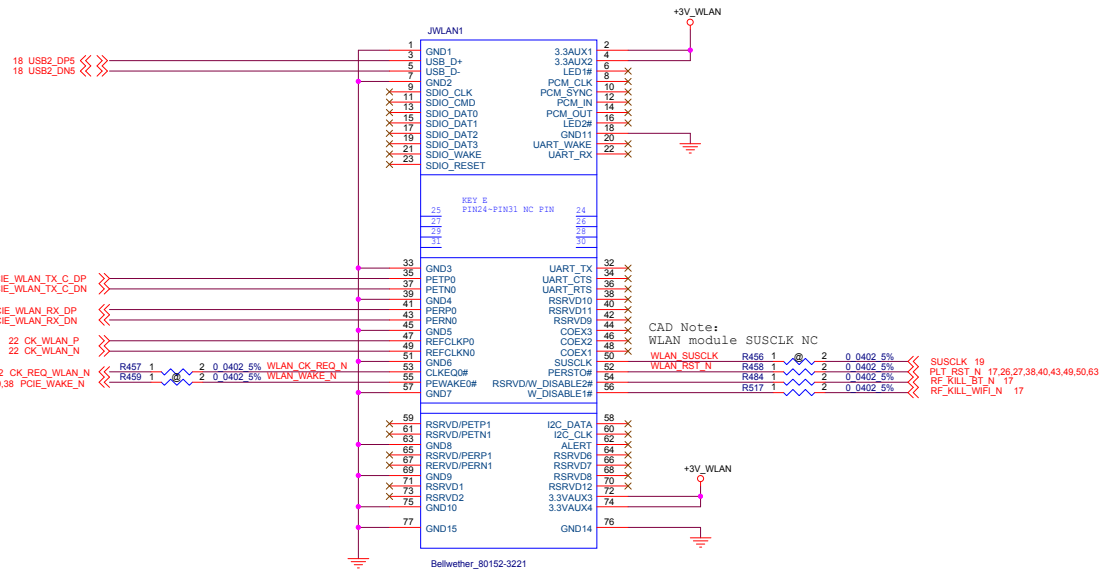
CAD Note: USB_CHG_CTL*
CLT1 CLT2 CLT3 ILIM_SEL
0 1 0 1 -- SDP
0 0 1 1-- DCP/Auto

CAD Note:
ILIM_SEL=Vin, ILIM_HI=22.6KR:
output current limit=2.3A

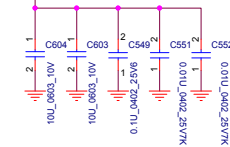
Support Mouse/Keyboard wake up.
Support Power Wake

CAD Note: For Power consumption

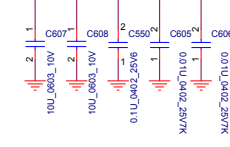


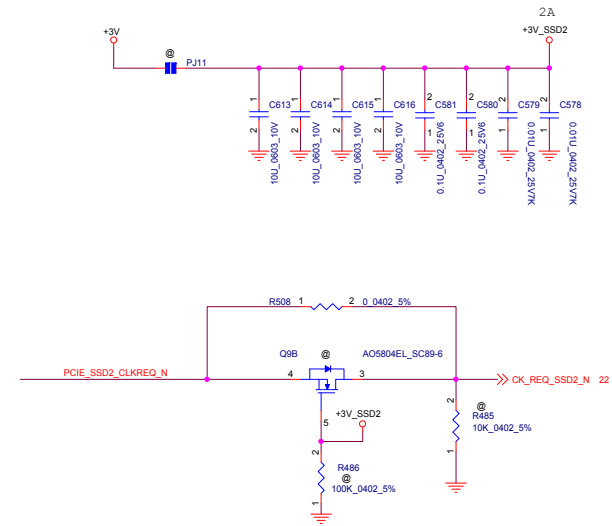
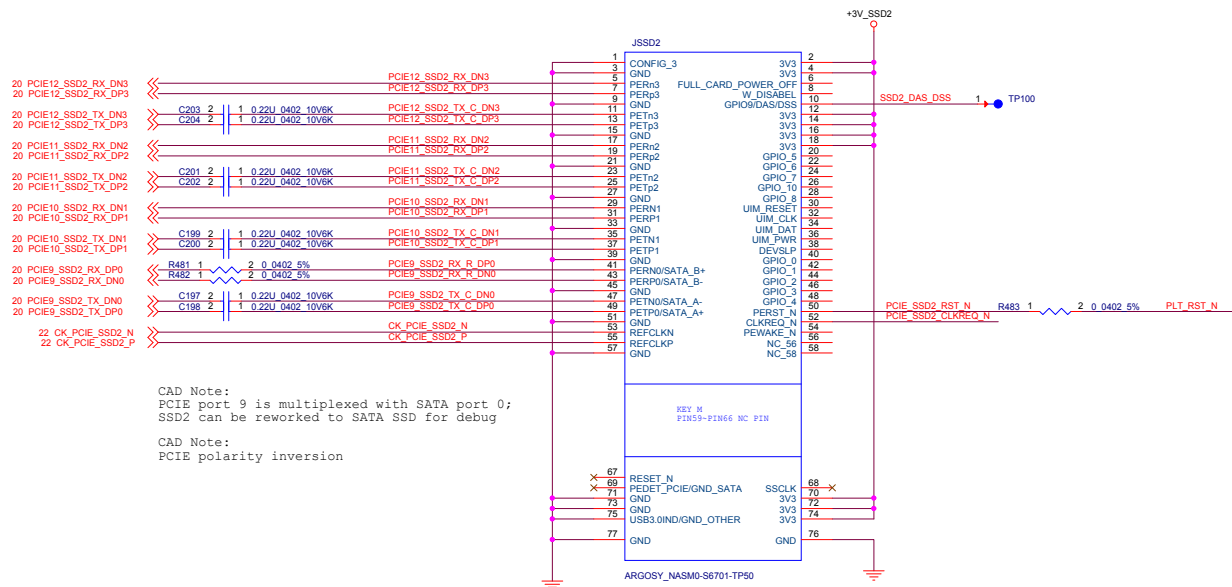
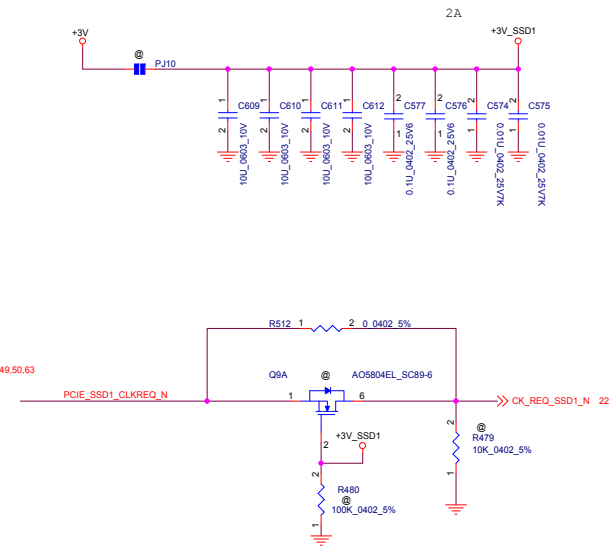
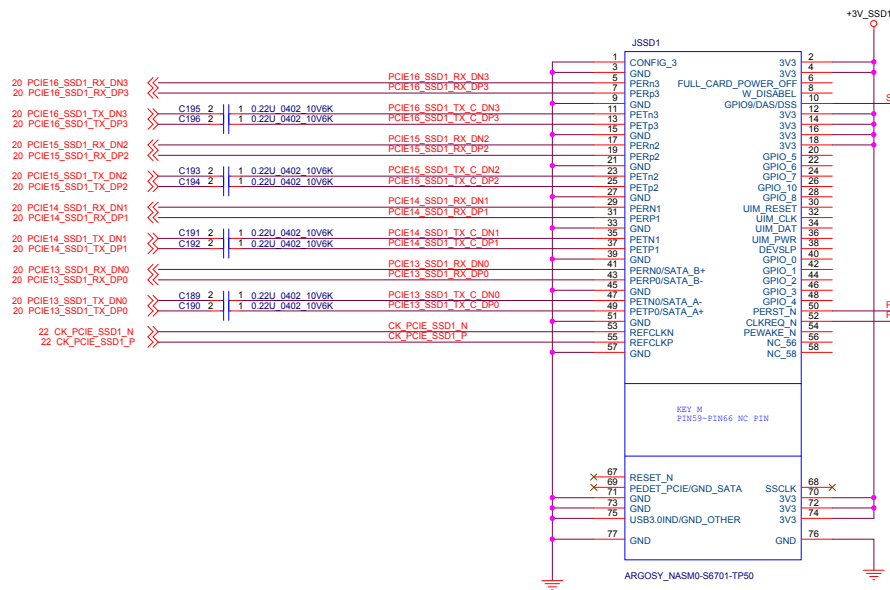


BRD Note:
Placed close to pin2,4



BRD Note:
Placed close to pin72,74

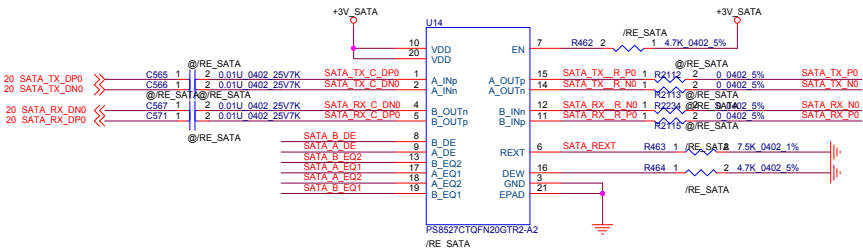
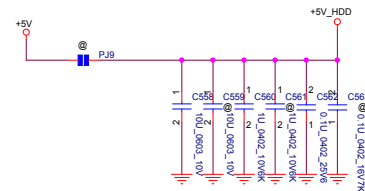
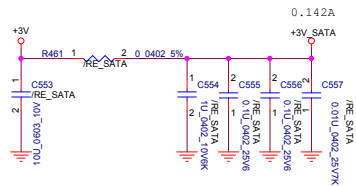




CAD Note:
PCIe port 9 is multiplexed with SATA port 0;
SSD2 can be reworked to SATA SSD for debug

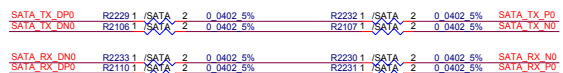
CAD Note:
PCIe polarity inversion

CAD Note: PS8527A VDD
1.2V/1.35V/1.5V



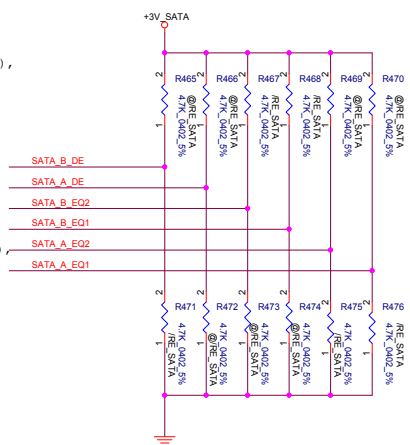
CAD Note:
SATA_REXT=7.5KR:
Vtx_diff=700 mV

CAD Note: SATA_DEW
L:For SATA Gen3
H:For SATA Gen2

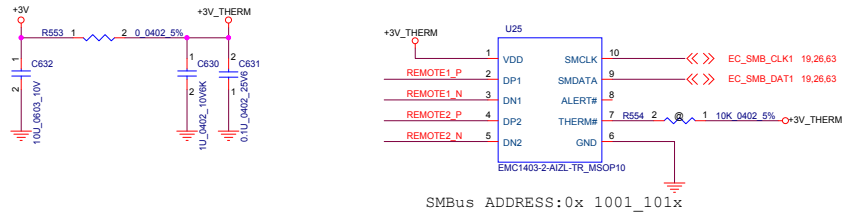


CAD Note: SATA_x_DE
De-emphasis level setting for channel x(x=A,B),
internally tied to VDD/2
[A_DE, B_DE]=M, L
M: -3.5dB
L: 0dB
H: -6dB

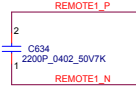
CAD Note: SATA_x_EQ
Equalization level setting for channel x(x=A,B),
internally tied to VDD/2
[x_EQ2, x_EQ1]=
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB (CH A)
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB (CH B)



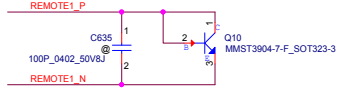
Theamal Sensor



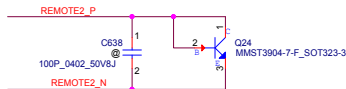
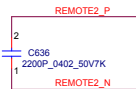
BRD Note:
Placed close to EMC1403



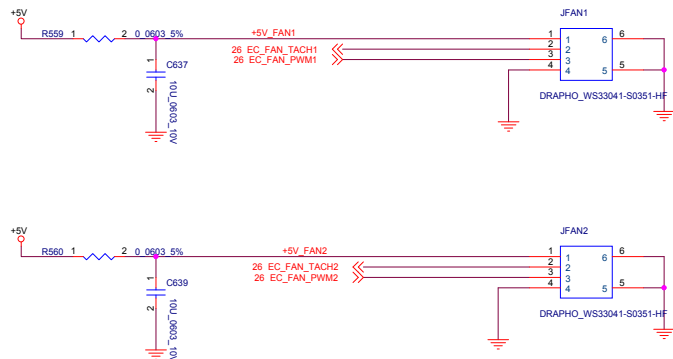
BRD Note:
Placed close to DDR
W/S=10:10



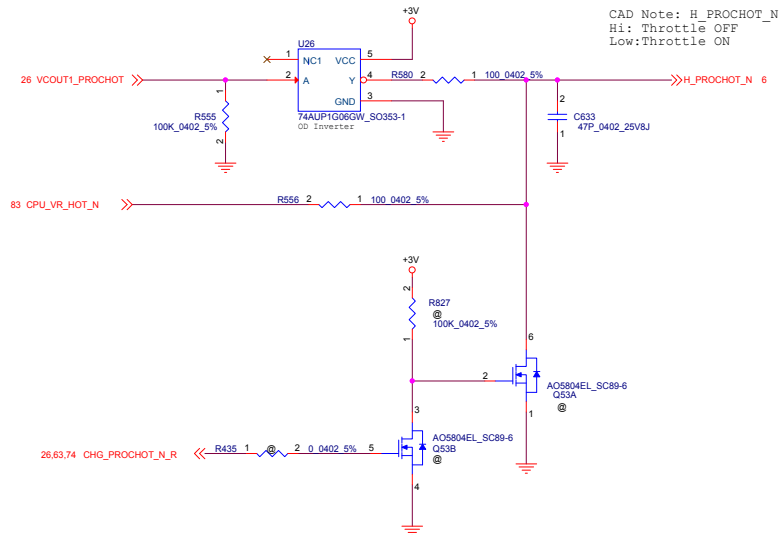
BRD Note:
Placed close to FAN



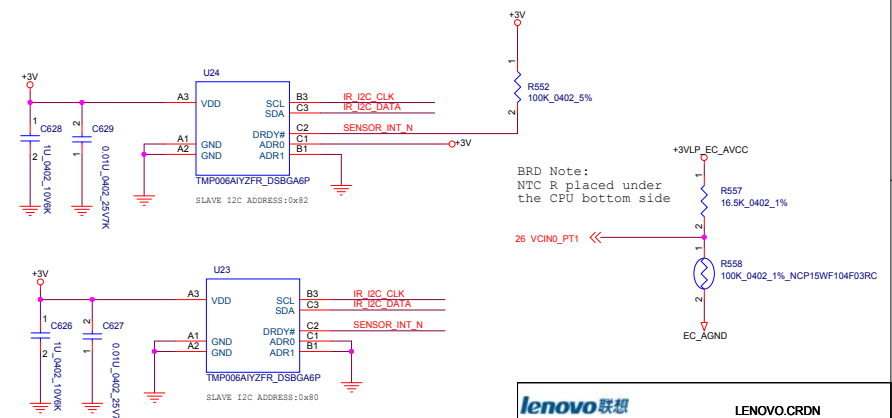
FAN CONN.



PROCHOT_N Logic

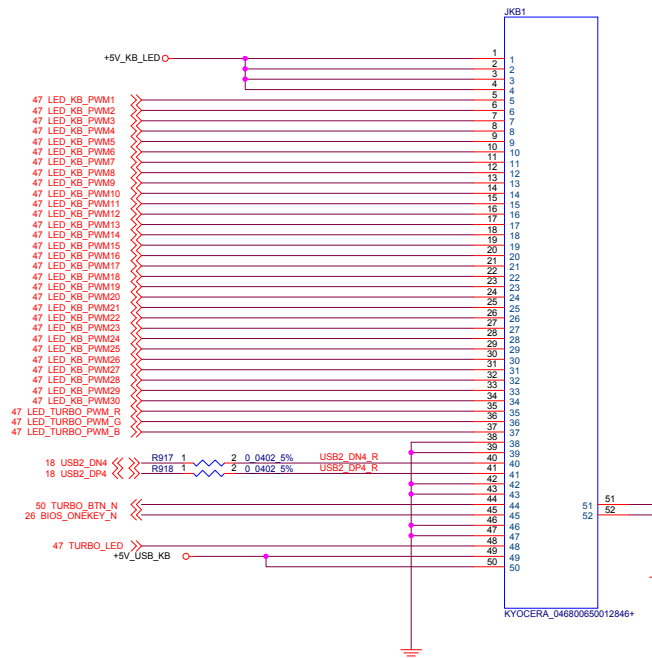
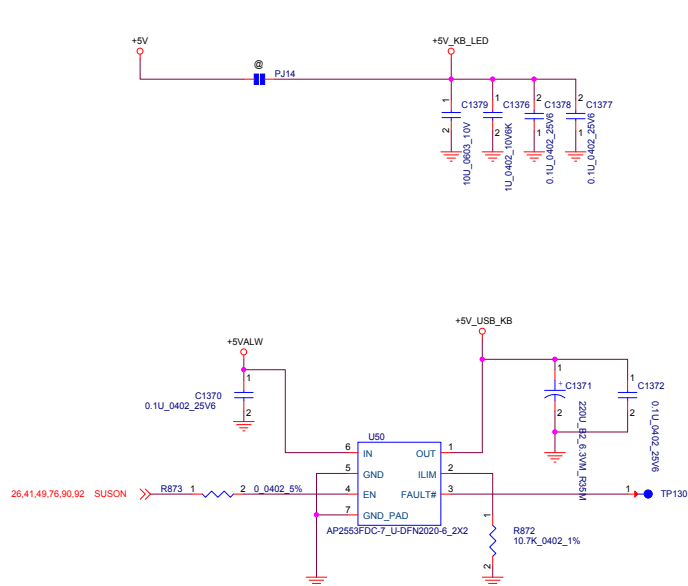


IR Sensor

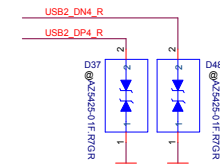


26.28 EC_I2C_CLKS <<< R550 1 2 0 0402 5% IR_I2C_CLK
26.28 EC_I2C_DATA5 <<< R551 1 2 0 0402 5% IR_I2C_DATA

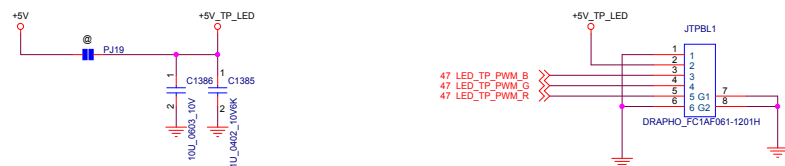
lenovo 联想		LENOVO.CRDN	
Title		Thermal/IR Sensor/FAN	
Size		Document Number	
C		Skylake-H	
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KB CONN.



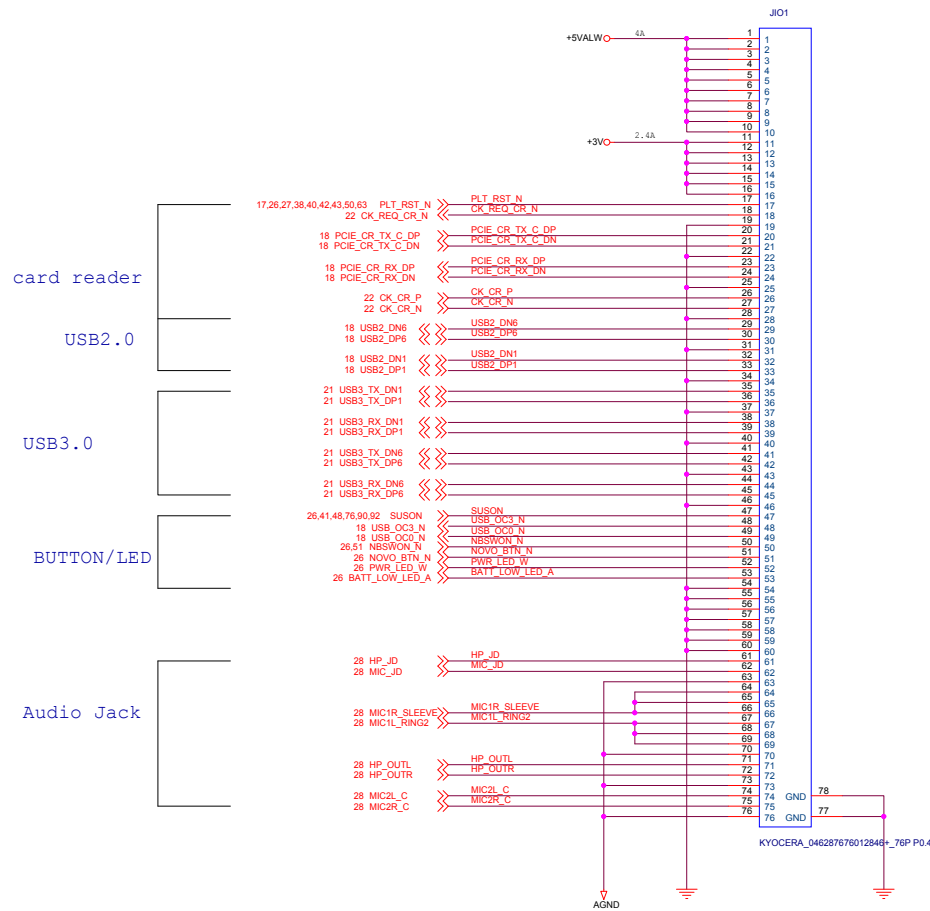
TP LED CONN.



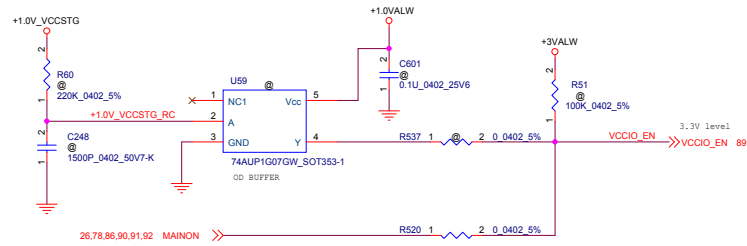
SPKR LED CONN.



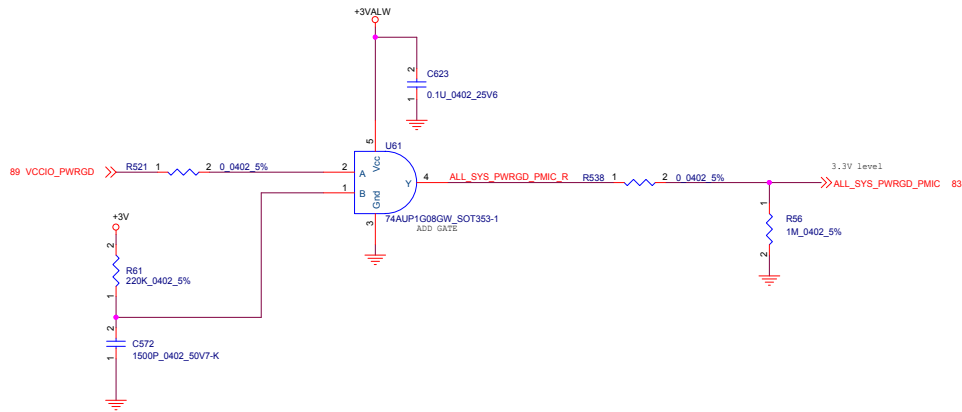
lenovo 联想		LENOVO.CRDN	
File KB/BACKLIGHT LED			
Size C	Document Number Skylake-H	Rev V0.3	
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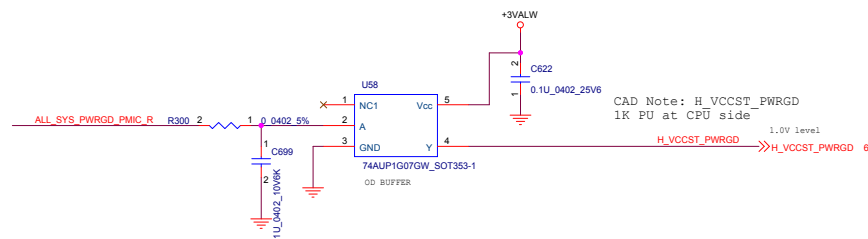
VCCIO_EN



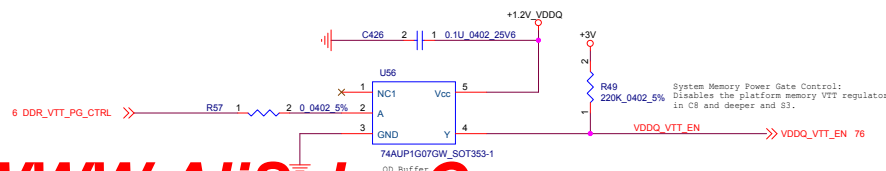
ALL_SYS_PWRGD_PMIC



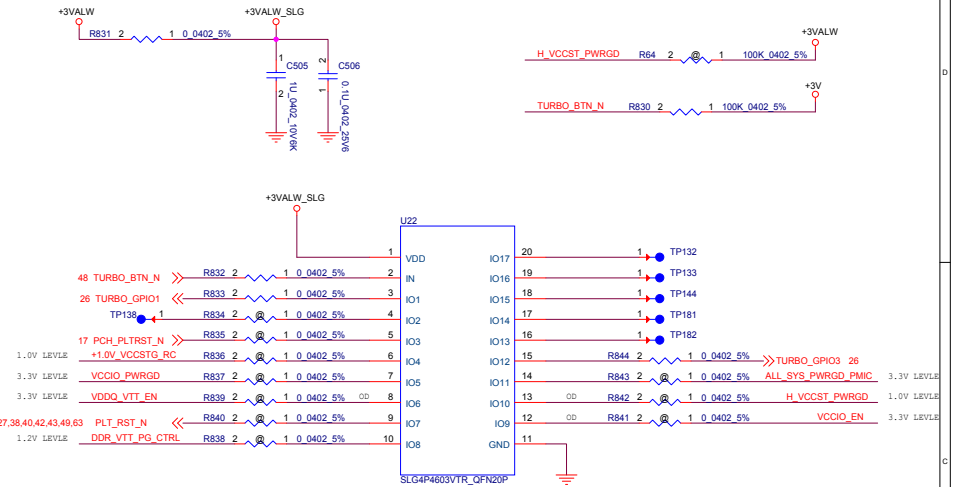
H_VCCST_PWRGD



VDDQ_VTT_EN

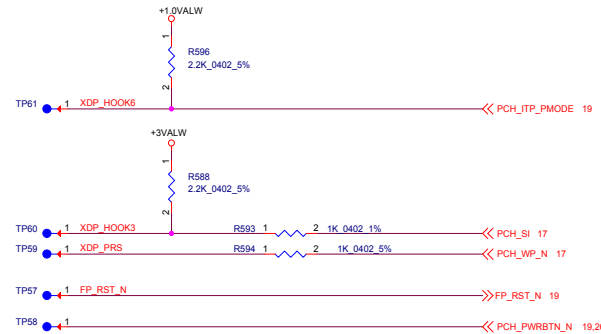
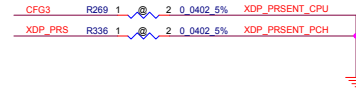
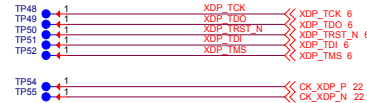
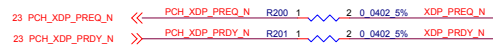
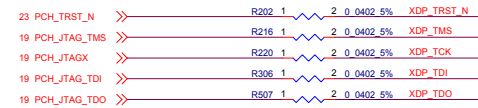
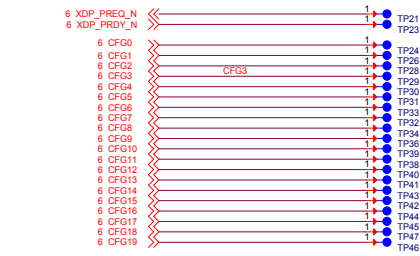


SLG4P4603VTR



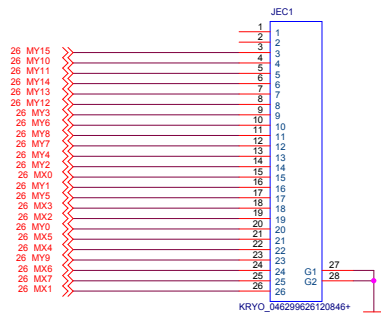
lenovo 联想		LENOVO.CRDN	
File			
PWRGD CONTROL			
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XDP CONN.



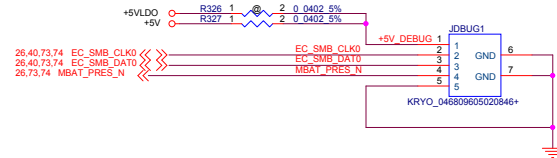
EC Debug CONN.

CAD Note:
For EC flash and debug



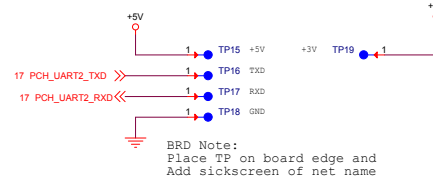
80 Port Debug CONN.

CAD Note:
For 80 port debug

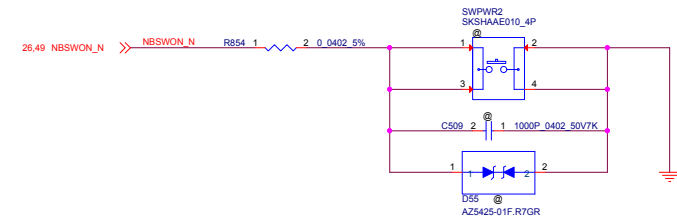


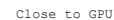
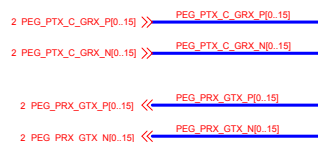
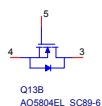
PCH UART Debug CONN.

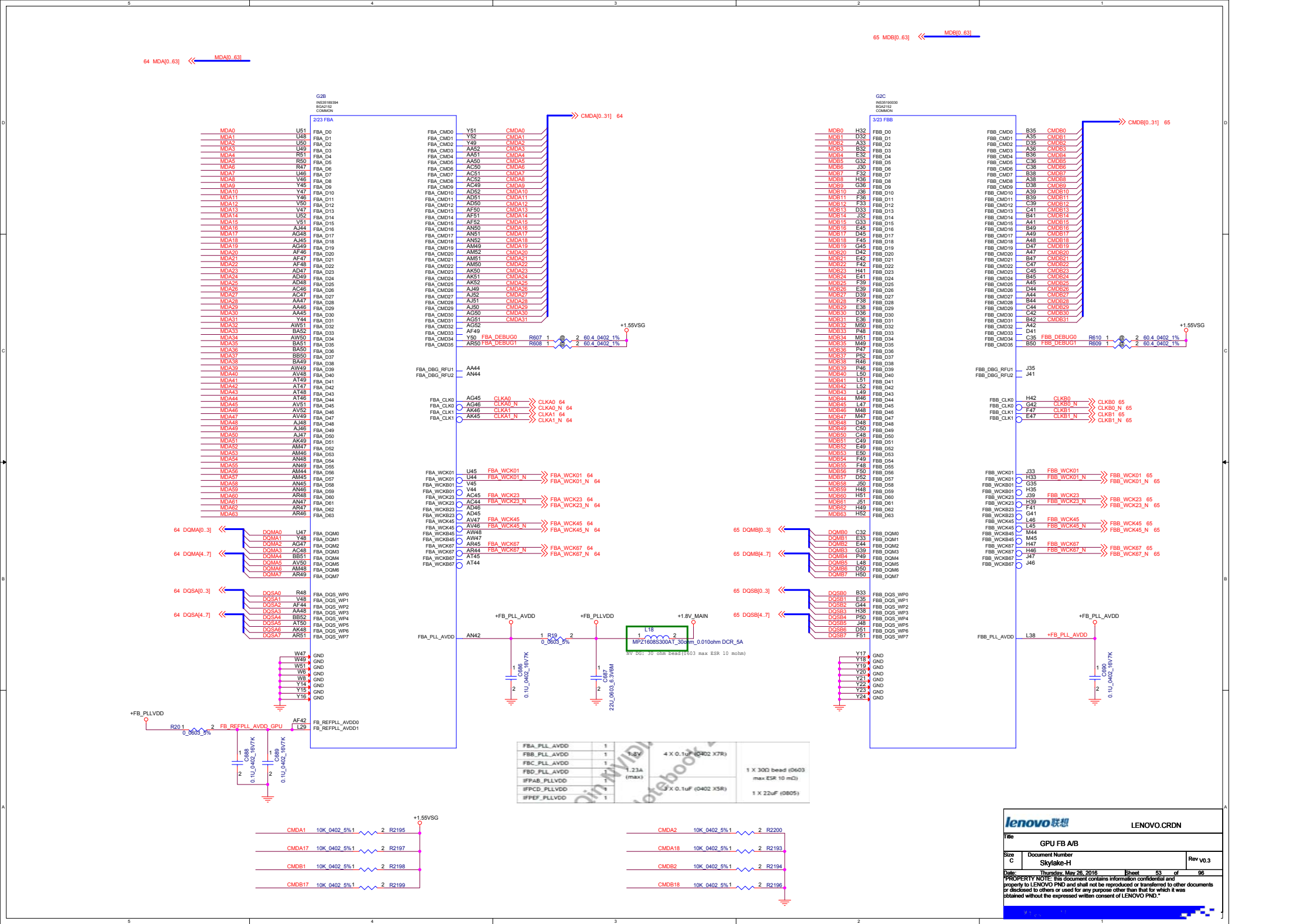
CAD Note:
For PCH UART port debug

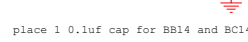


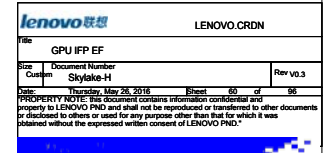
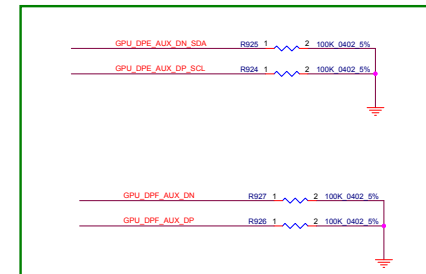
MB PWRBTN

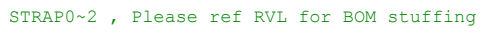
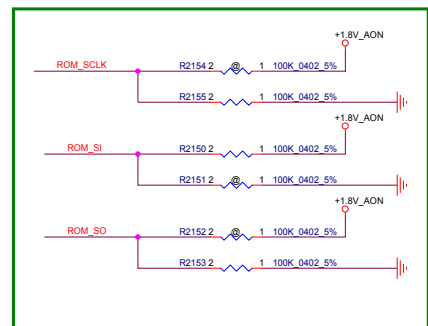
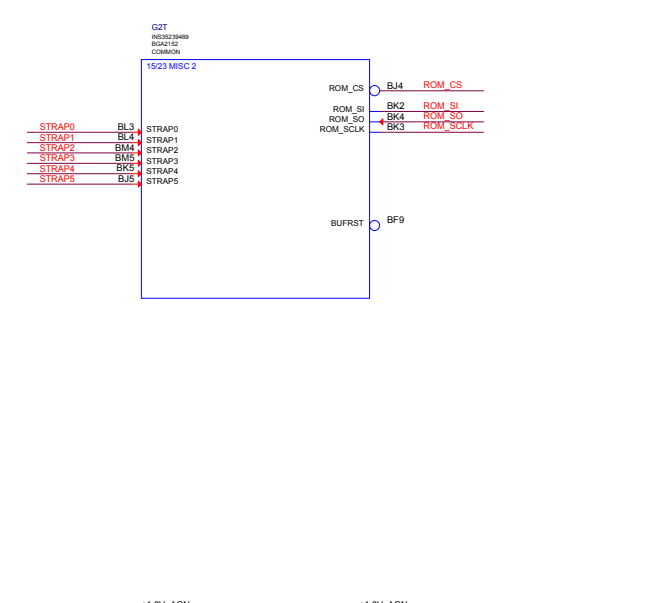







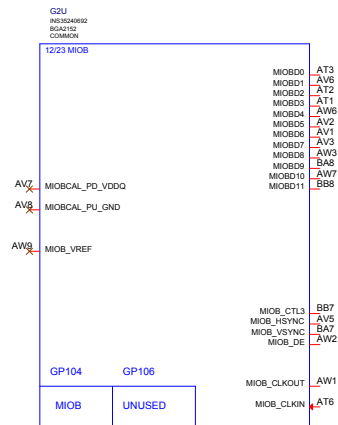
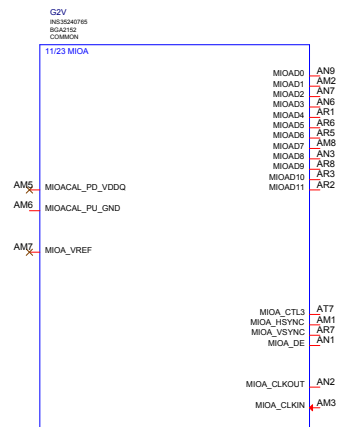


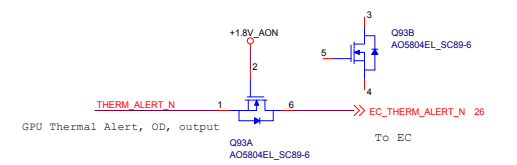
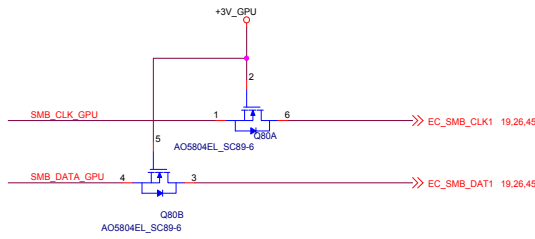
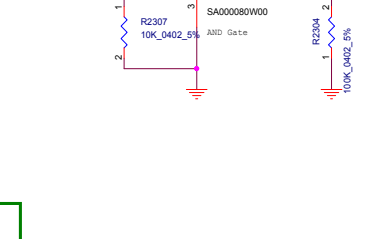
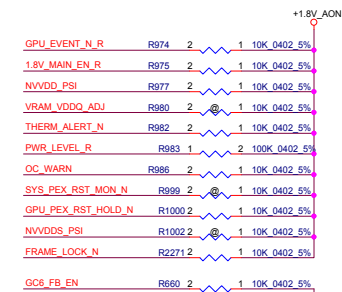
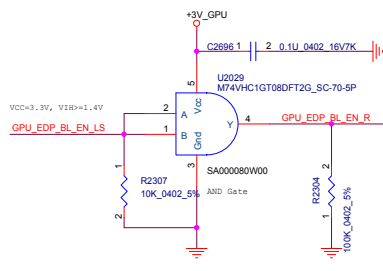
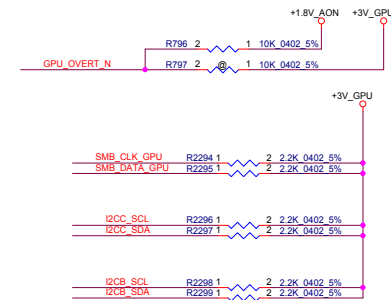




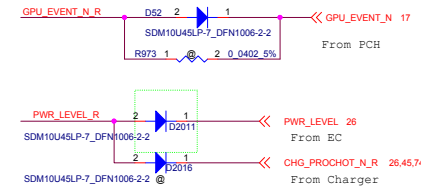
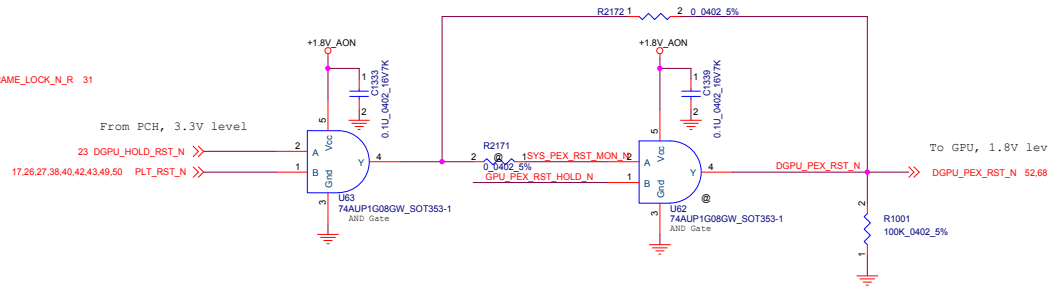
ROM_SCLK(LSB)/ROM_SI/ROM_SO(MSB) :							
Row Index	Strap Pins <i>see Note</i>			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED

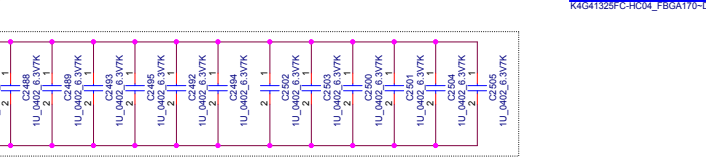
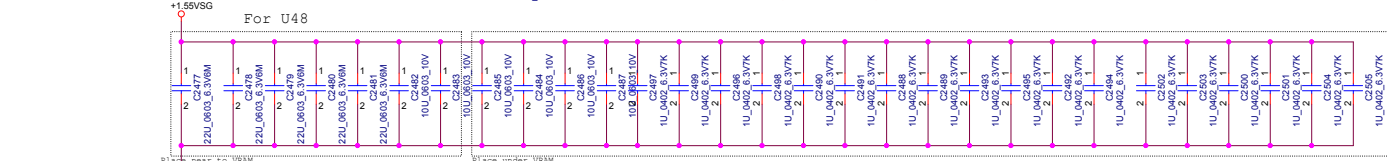
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Title GPU PLI/XTAL			
Size C	Document Number SkyLake-H		Rev V0.3
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The schematic diagram shows the internal circuitry of the AO5804EL_SC89-6 driver. It features a +3V_EDP supply connected to a 10K resistor R784, which is in series with a 0.1uF capacitor C885. The output of the capacitor is connected to the gate of MOSFET Q48A. The gate of Q48A is also connected to a 10K resistor R781, which is connected to the GPU_EDP_VDD_EN_LS input. The source of Q48A is connected to ground. The drain of Q48A is connected to the FRAME_LOCK_N output. The gate of MOSFET Q48B is connected to the FRAME_LOCK_N output. The source of Q48B is connected to ground. The drain of Q48B is connected to the FRAME_LOCK_N output. The MOSFETs are AO5804EL_SC89-6.







54 MDC[0..63] >>> MDC[0..63]
54 CMDQ[0..31] >>> CMDQ[0..31]
54 DQM[0..7] >>> DQM[0..7]
54 DQSC[0..7] >>> DQSC[0..7]

MIRROR

54 CLKC0 >>> CLKC0 R2226 2 1 40.2 0402 1%
54 CLKC0_N >>> CLKC0_N R2227 2 1 40.2 0402 1%

0.01U_0402_25V7K
C1353

+1.55VSG
R900 1 2 1K 0402 1%
J1
MF
SEN
ZQ

2 R998 1 121 0402 1%
FBC_ZQ_1_B J13

54 FBC_WCK23_N >>> FBC_WCK23_N D5
54 FBC_WCK23 >>> FBC_WCK23 D4
54 FBC_WCK01_N >>> FBC_WCK01_N P5
54 FBC_WCK01 >>> FBC_WCK01 P4

A10
U10
VREFD
VREFC
J14

C1354 1 820P 0402 50V7K
FBC_VREFC

CMDC2 J2 RESET#

+1.55VSG
G1
L1
G4
VDD
G5
VDD
C8
VDD
C10
VDD
R10
VDD
G11
VDD
G14
VDD
L14
VDD

R997 549 0402 1%
R895 1.33K 0402 1%
FBC_VREFC

931 0402 1%
R2224
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

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NORMAL

54 CLKC1 >>> CLKC1 R903 2 1 40.2 0402 1%
54 CLKC1_N >>> CLKC1_N R901 2 1 40.2 0402 1%

0.01U_0402_25V7K
C2425

+1.55VSG
R904 1 2 1K 0402 1%
J1
MF
SEN
ZQ

2 R998 1 121 0402 1%
FBC_ZQ_2_B J13

54 FBC_WCK45_N >>> FBC_WCK45_N D5
54 FBC_WCK45 >>> FBC_WCK45 D4
54 FBC_WCK67_N >>> FBC_WCK67_N P5
54 FBC_WCK67 >>> FBC_WCK67 P4

A10
U10
VREFD
VREFC
J14

C1355 1 820P 0402 50V7K
FBC_VREFC

CMDC18 J2 RESET#

+1.55VSG
G1
L1
G4
VDD
G5
VDD
C8
VDD
C10
VDD
R10
VDD
G11
VDD
G14
VDD
L14
VDD

R997 549 0402 1%
R895 1.33K 0402 1%
FBC_VREFC

931 0402 1%
R2224
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

VRAM_VREF_CTI >>> 63.64 6597
Q83A 2
Q83B 3
Q83C 5
Q83D 6
Q83E 7
Q83F 8
Q83G 9
Q83H 10
Q83I 11
Q83J 12
Q83K 13
Q83L 14

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GPU VRAM C

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Thursday, May 26, 2016

Sheet

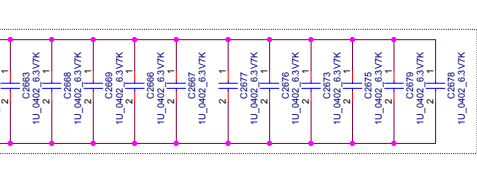
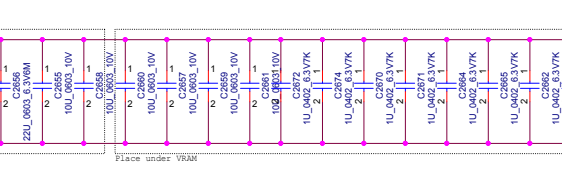
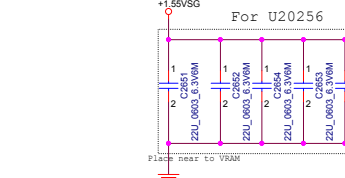
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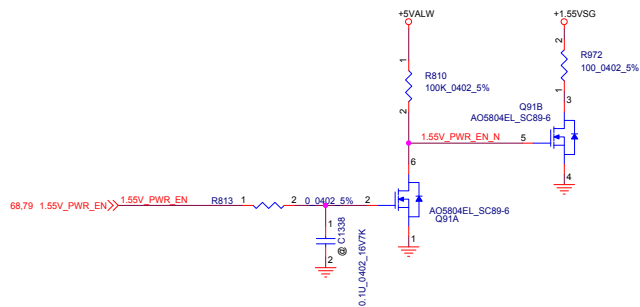
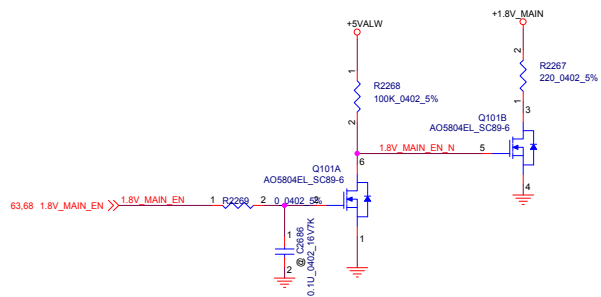
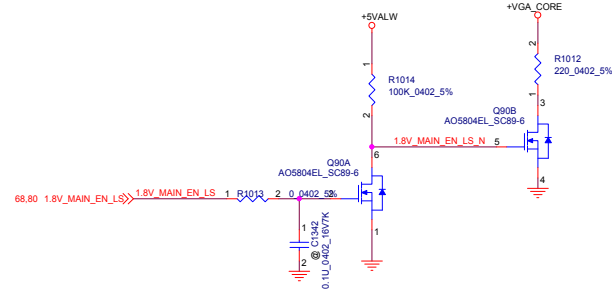
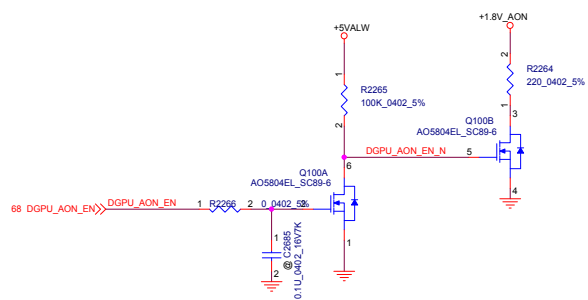
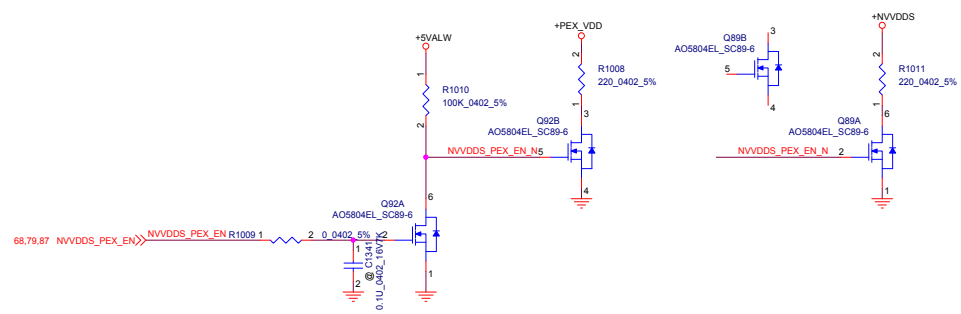
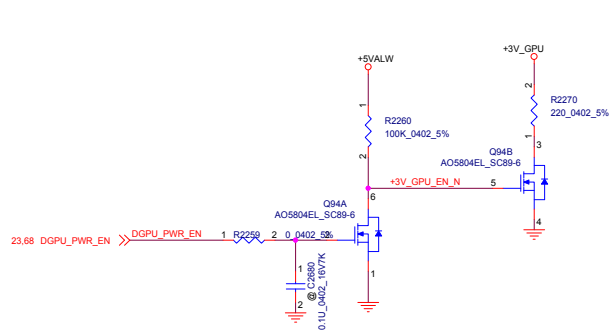
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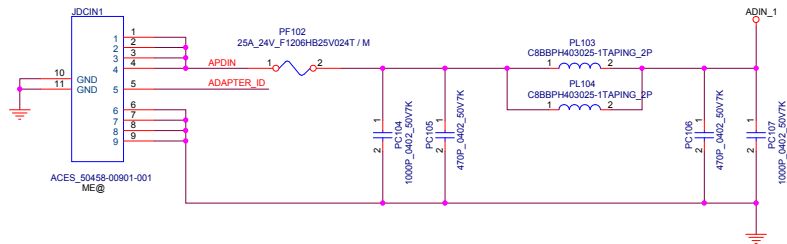
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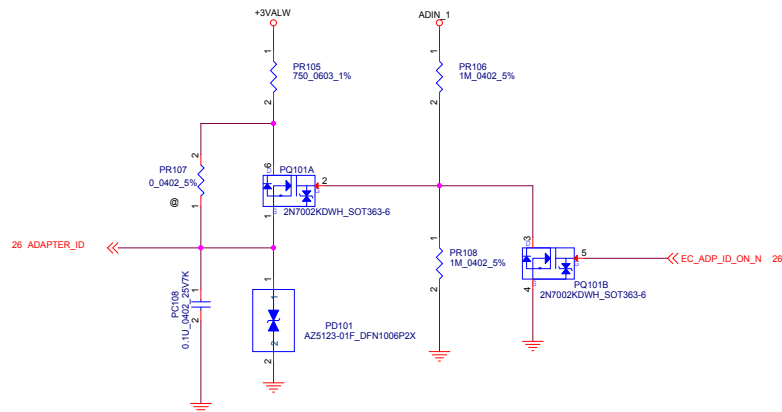
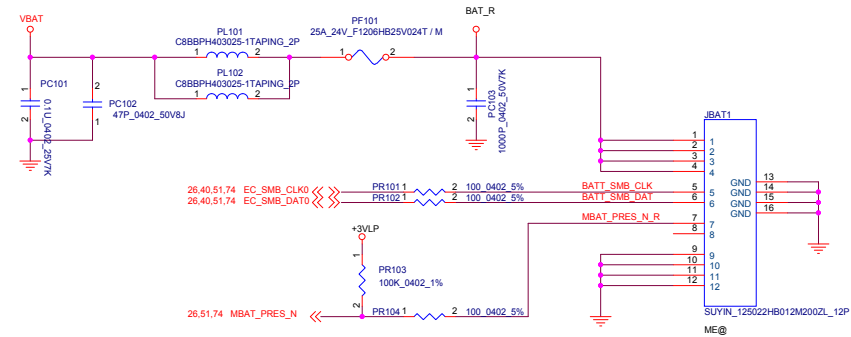
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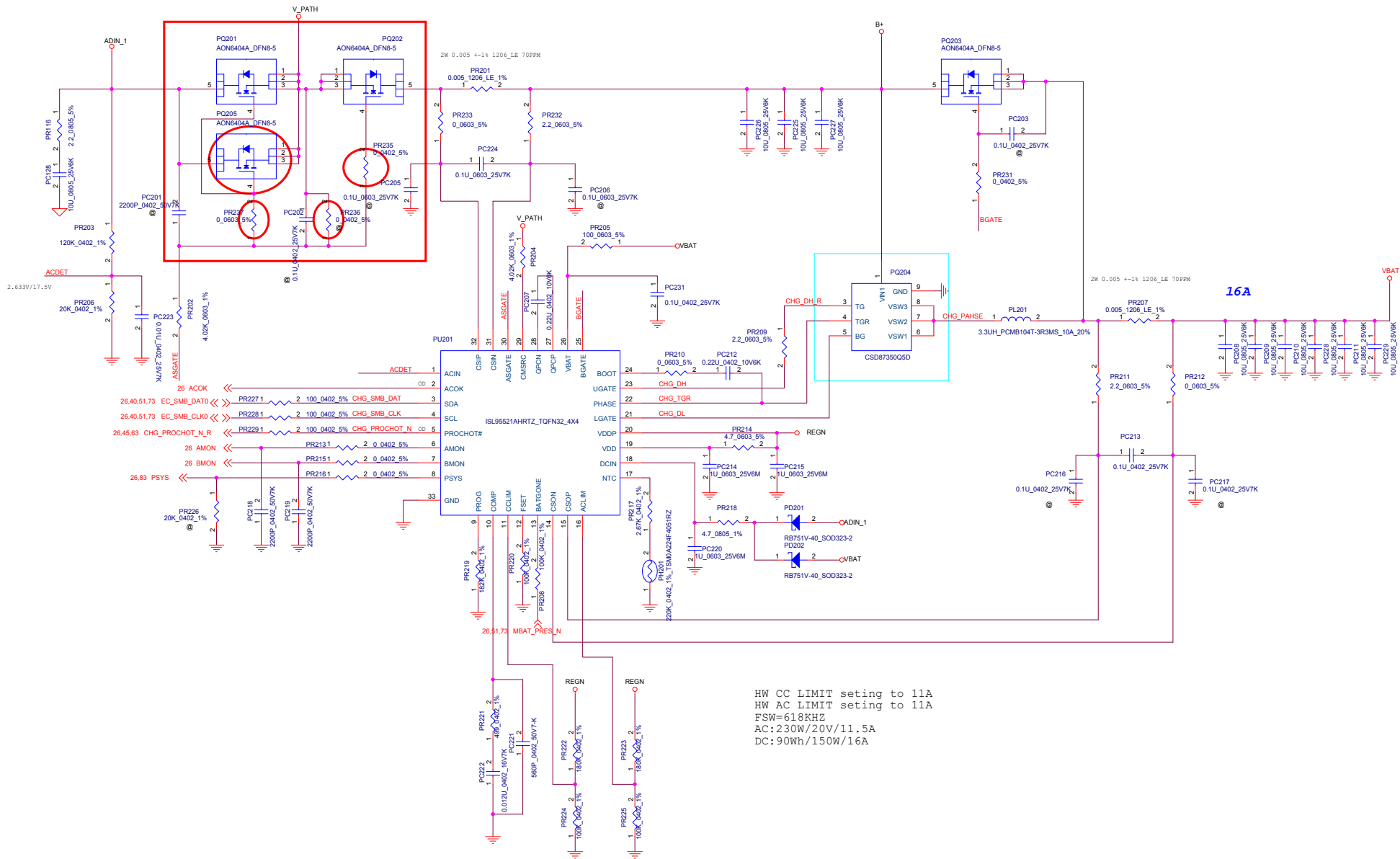


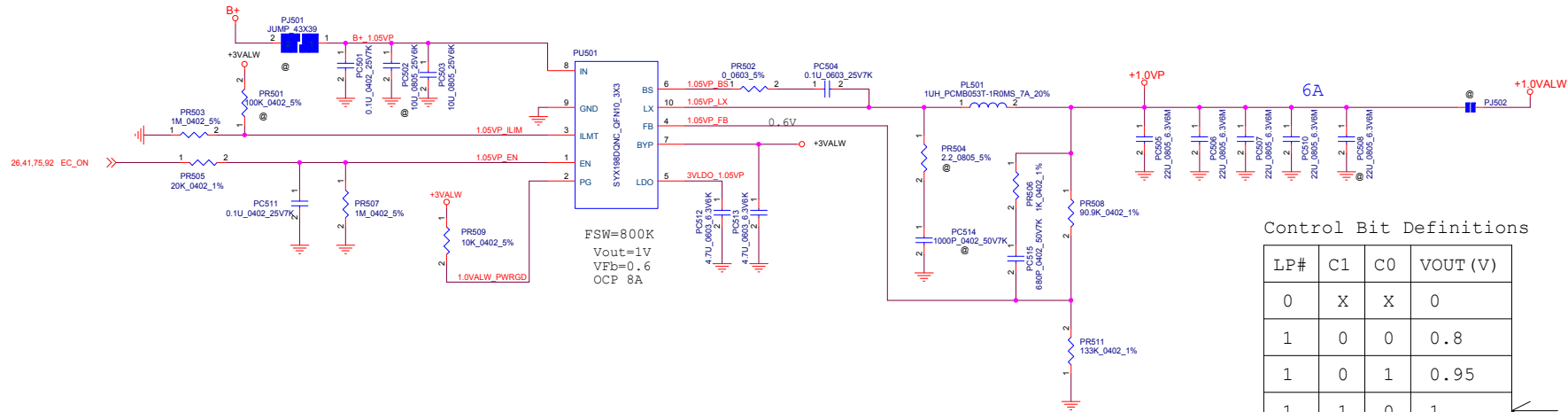
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	Skylake-H				
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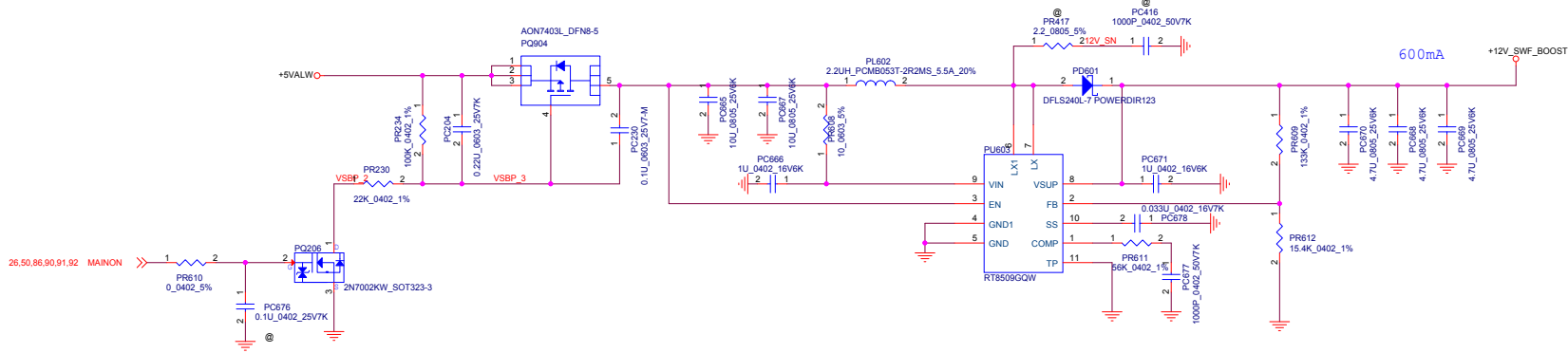
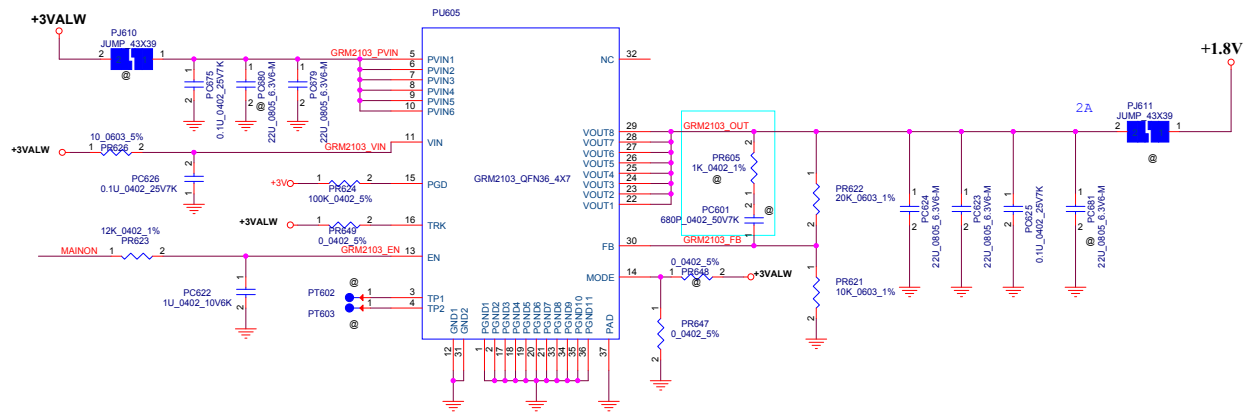


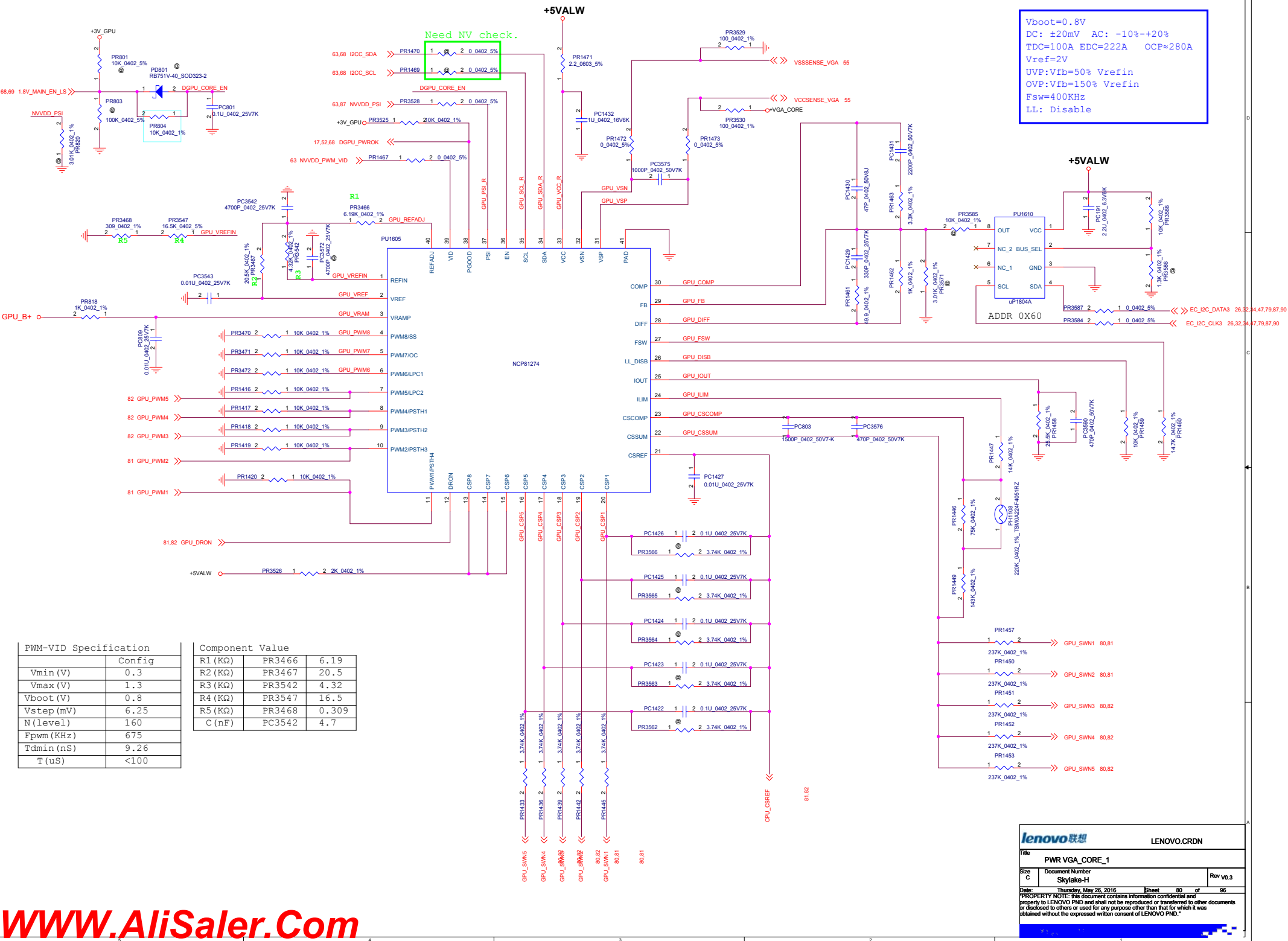




Control Bit Definitions

LP#	C1	C0	VOUT (V)
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1
1	1	1	1.05





PWM-VID Specification	
Config	
Vmin (V)	0.3
Vmax (V)	1.3
Vboot (V)	0.8
Vstep (mV)	6.25
N (level)	160
Fpwm (KHz)	675
Tdmin (nS)	9.26
T (uS)	<100

Component Value			
R1 (KΩ)	PR3466	6.19	
R2 (KΩ)	PR3467	20.5	
R3 (KΩ)	PR3542	4.32	
R4 (KΩ)	PR3547	16.5	
R5 (KΩ)	PR3468	0.309	
C (nF)	PC3542	4.7	

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Title

PWR VGA_CORE_1

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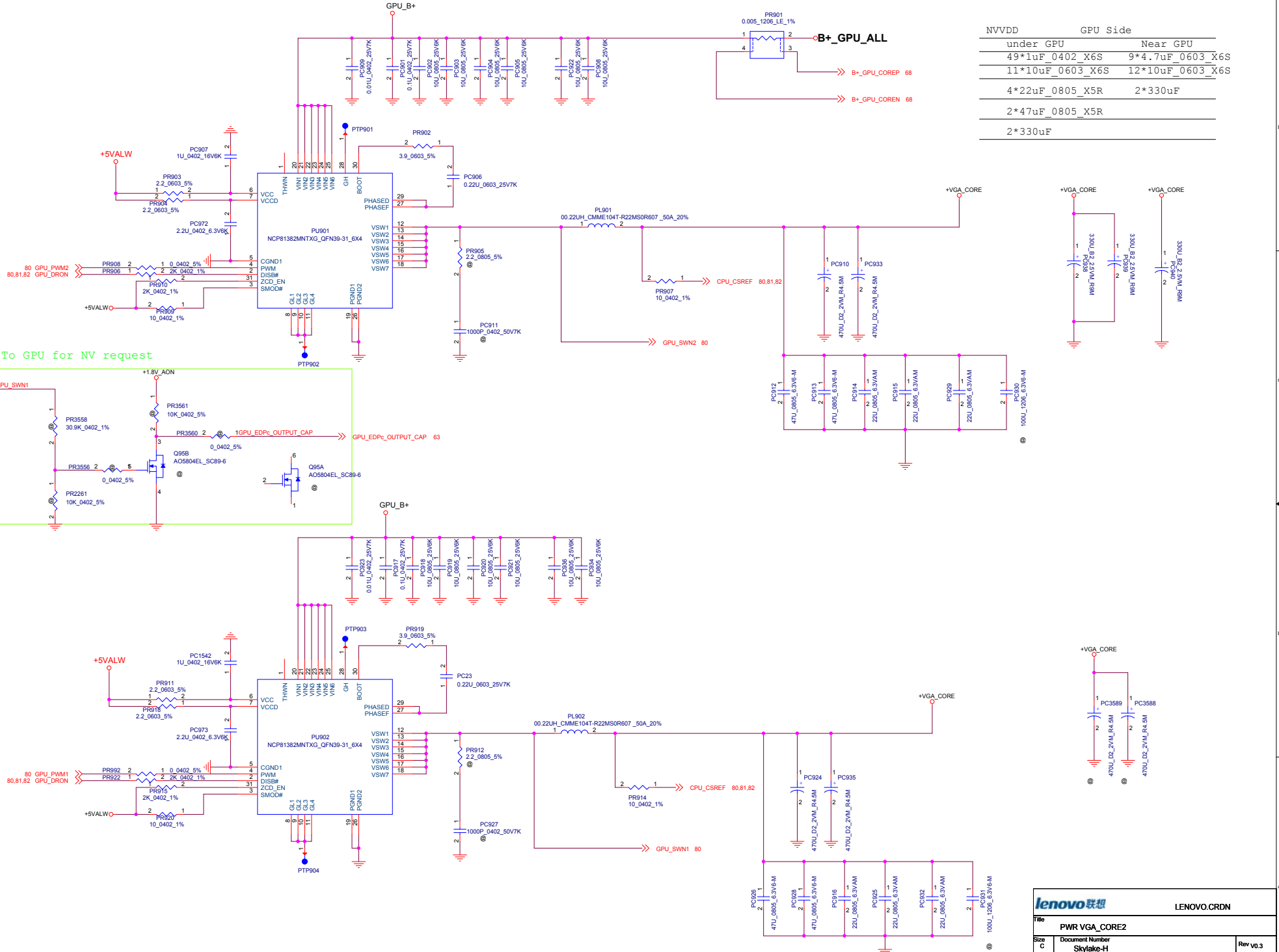
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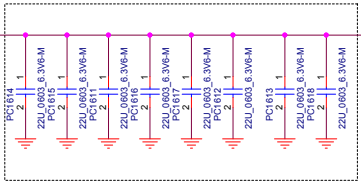
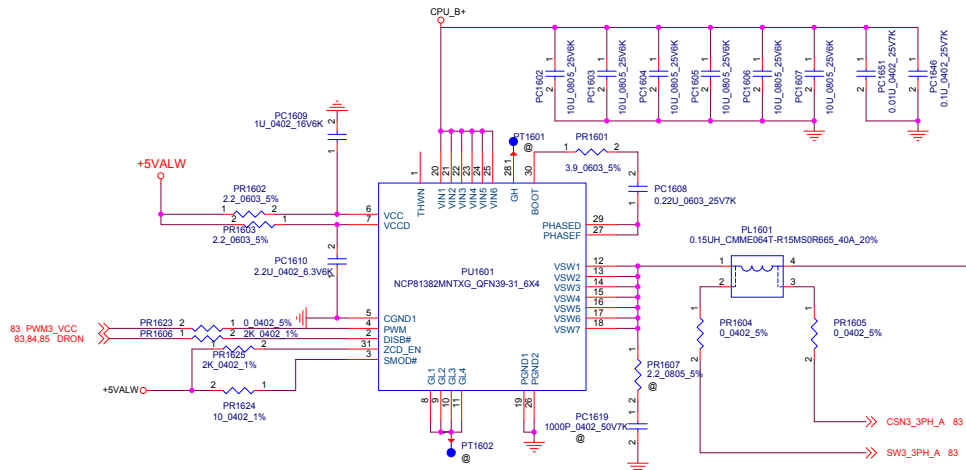
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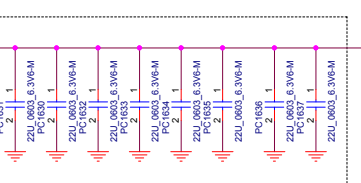
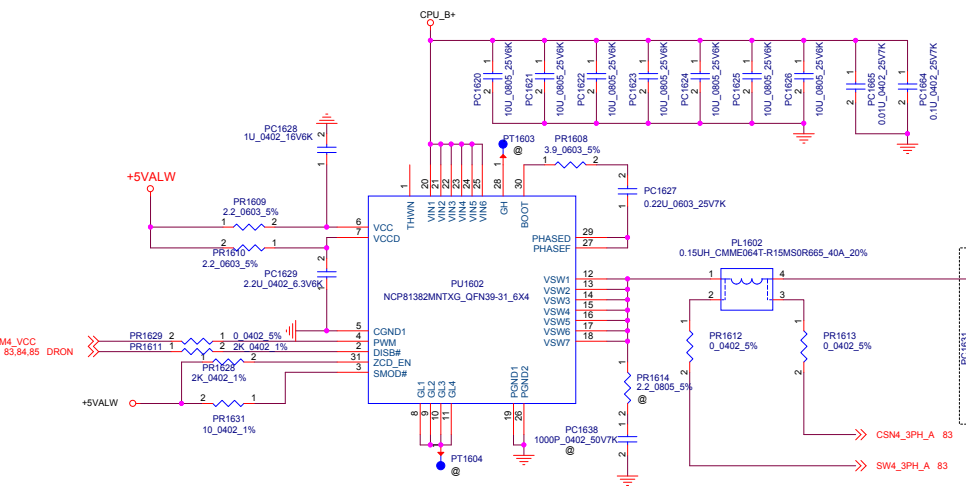
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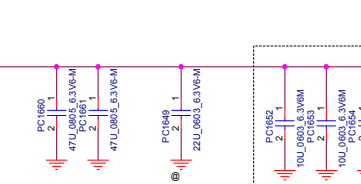
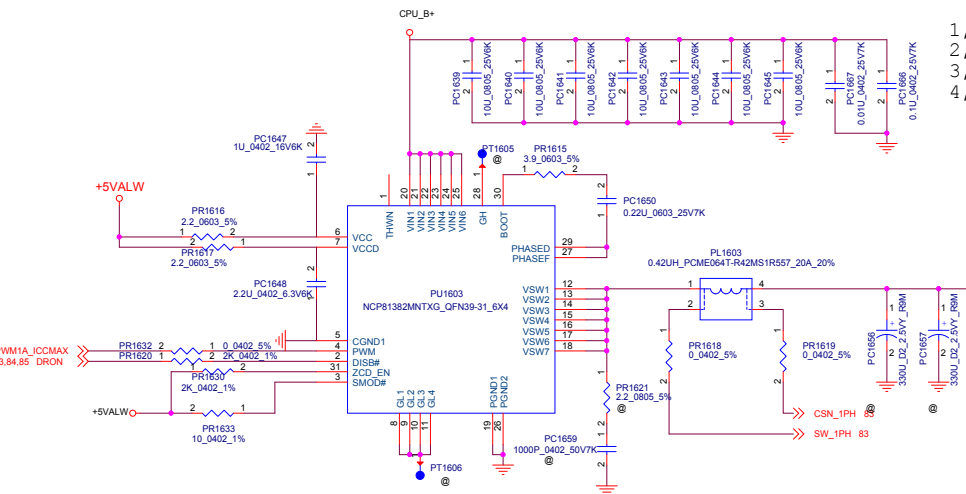




Board edge caps



Board edge caps



- 1,PDG 1*220uF TOP ,47uF*2; follow CRB/PDG;
- 2,47uF,22uF follow CRB;
- 3,1uF double check EE side
- 4,Total Cap double check with Vendor

VCCSA	CPU BACK				CPU TOP	
CRB	220	47	10	1	220	22
	2V	0805	0402	0201	2V	0603
pcs	0	1	7	3	2	1

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Title: PWR_CPU_CORE3(NCP81382)

Size: C

Document Number: SkyLake-H



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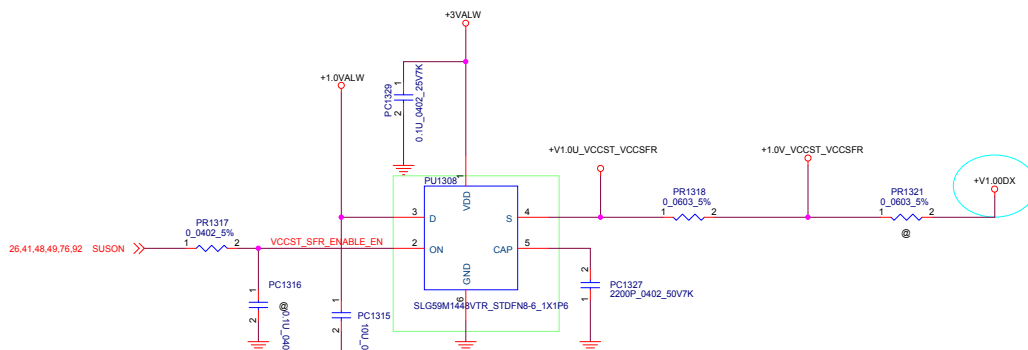
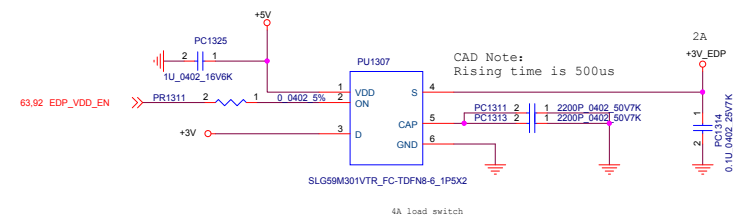
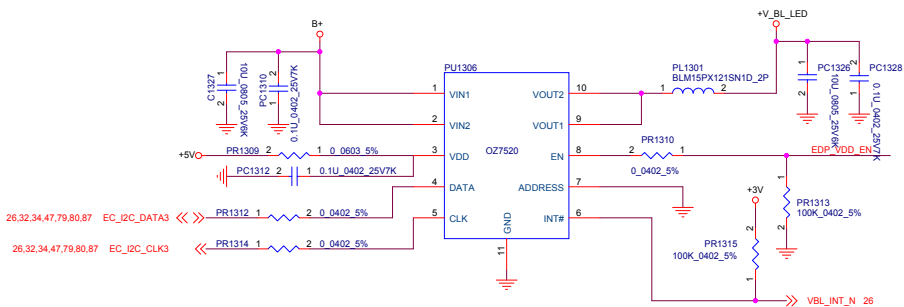
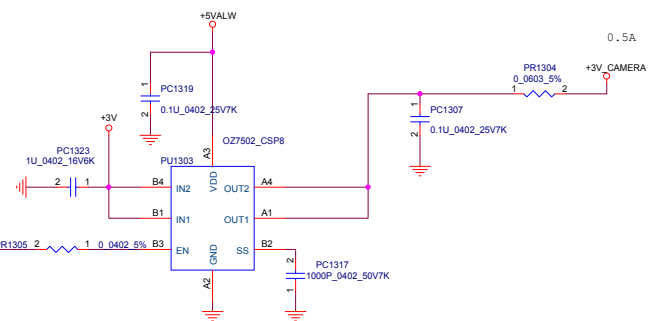
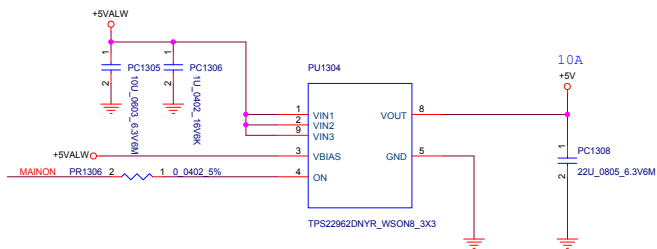
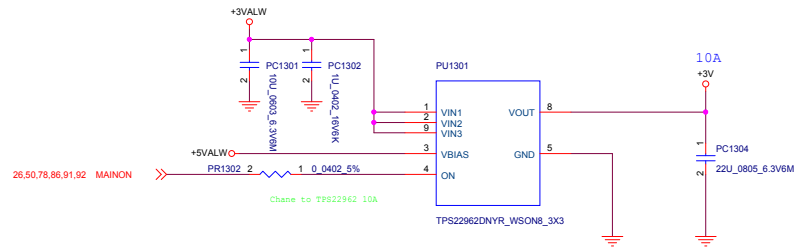
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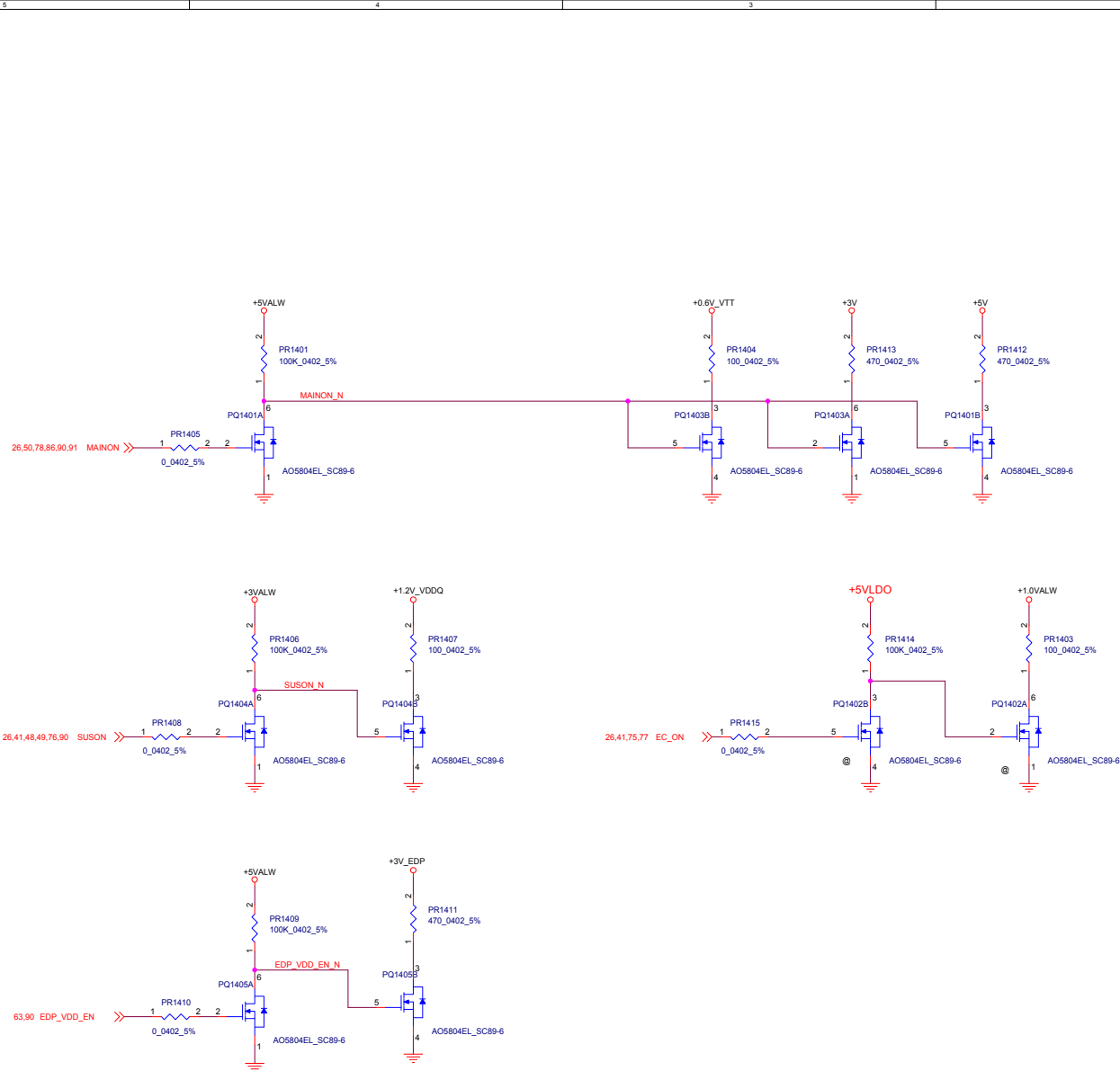
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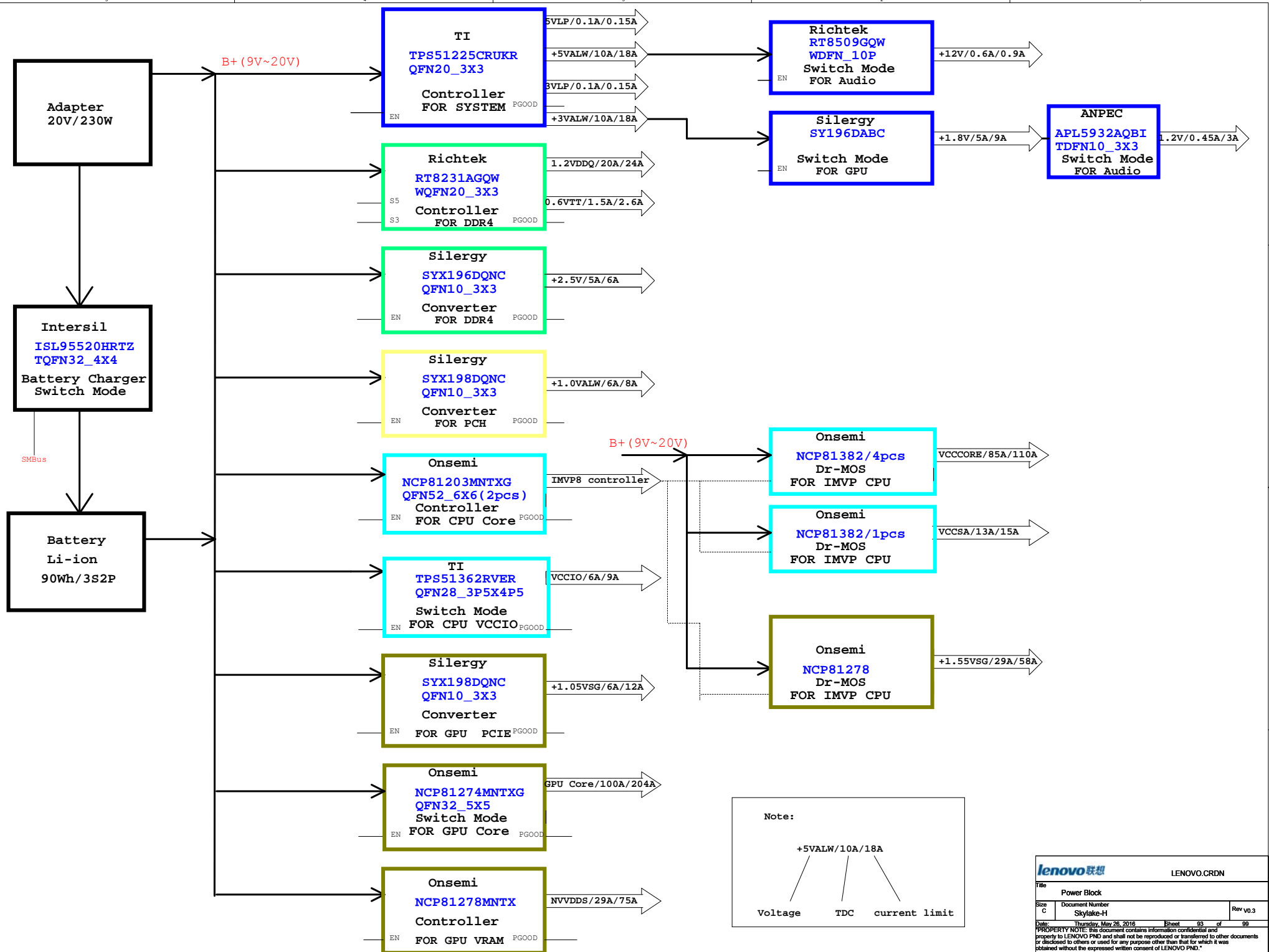


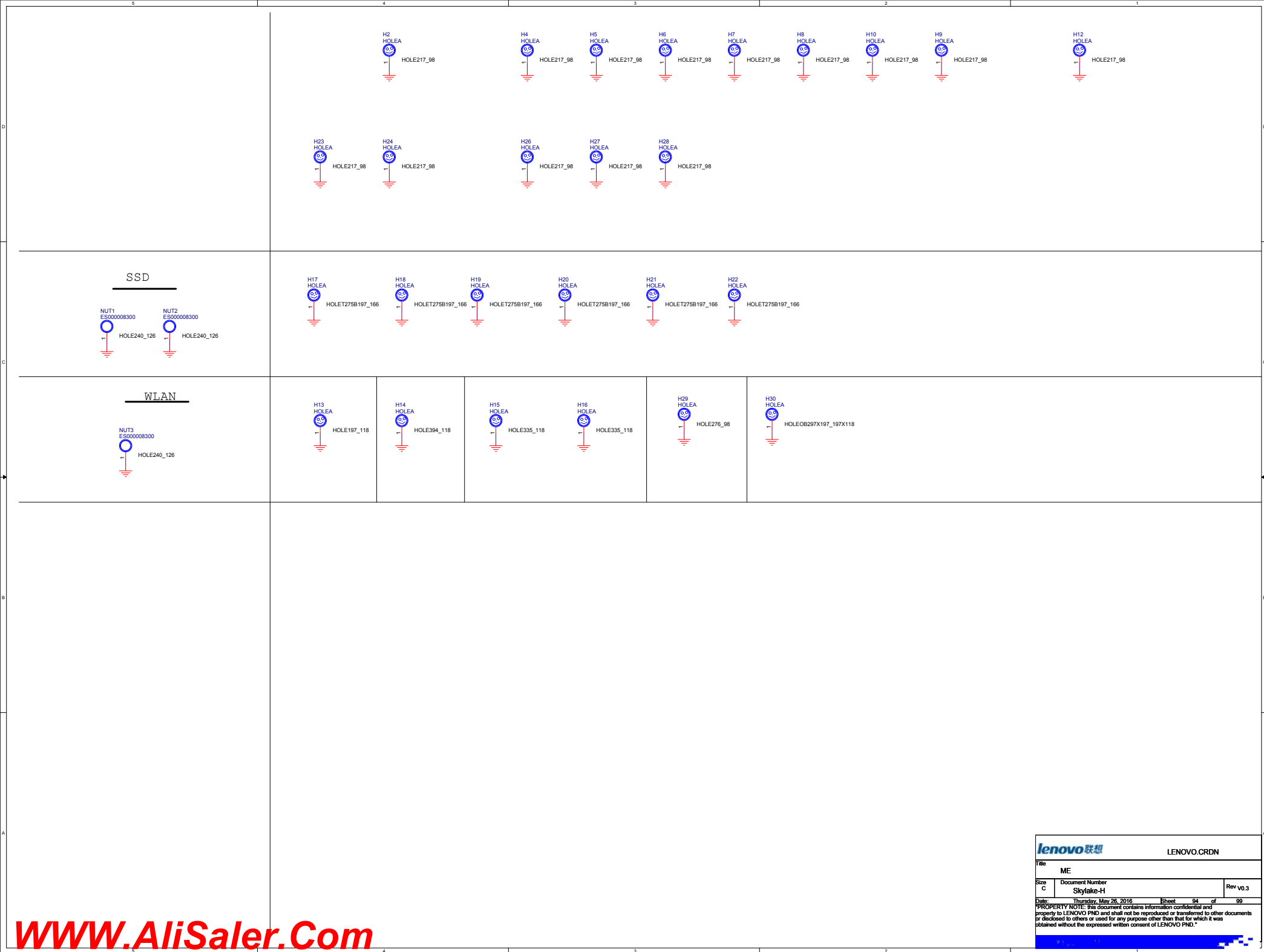
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Power switch1			
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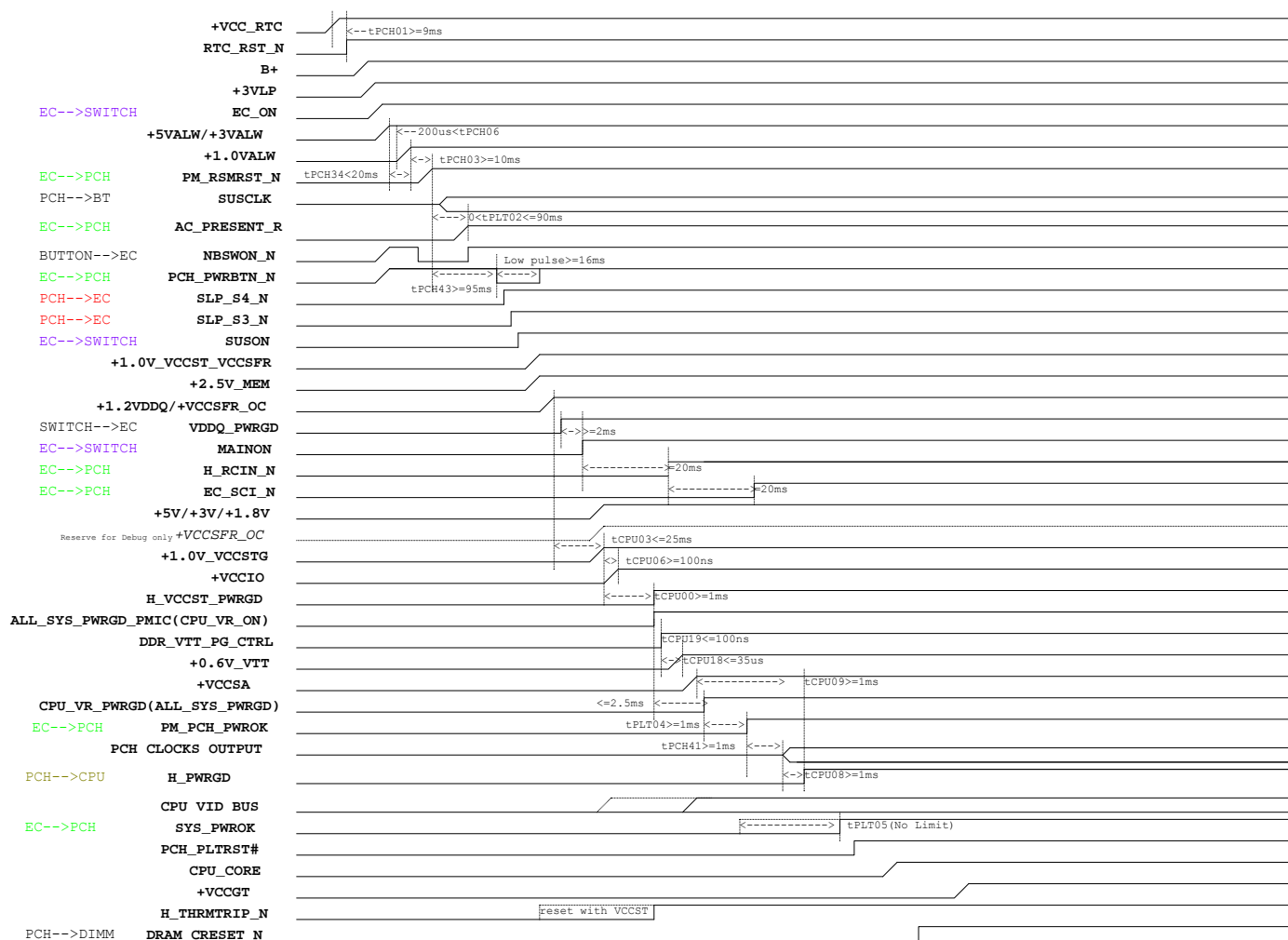
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G3-->S5/S4-->S0 (Non-Deep Sx platform)



5	4	3	2	1
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Flexible I/O

HSIO PORTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
CONFIGUR	USB3.0 PORT1		USB3.0 PORT3			USB3.0 PORT6	PCIE PORT1(1X4)					PCIE PORT6	PCIE PORT7	PCIE PORT8	PCIE PORT9(1X4)				PCIE PORT13(1X4)					SATA PORT6				
DEVICE	JUSB3(IO)		JUSB2			JUSB4(IO)	U2005(Intel AR DP)						Card Reader	WLAN	LAN	PCIE SSD2				PCIE SSD1					HDD			

SMBus Table

Master EC	Slave Device					
EC_SMB_CLK0 EC_SMB_DATA0	PJ201 CHARGER 0x 0001 001x	JBAT1 BATTERY 0x 16	U2007 TPS65982 0x			
EC_SMB_CLK1 EC_SMB_DATA1	U2 PCH	U25 Thermal Sensor 0x 1001 101x	G2 dGPU 0x 9E	J9C0M1 MXM 0x 9C		
EC_I2C_CLK3 EC_I2C_DATA3	U19 LC	PJ1255 TPS22993 0x 1110 010x	PJ1256 TPS22993 0x 1110 000x	PJ1306 OZ7520 0x 2E	U2019 PI3HDX1204BZHE 0XC2	U2015 PI3DPX1203ZHE 0XF2
EC_I2C_CLK5 EC_I2C_DATA5	U23 IR sensor 0x 1000 000x	U24 IR sensor TMP006 0x 1000 001x	U27 IR sensor 0x 1000 100x	U5002(reserve) RGB sensor CS5032 0x 1C	U8 (reserve) AMP TAS5766 0x 1001 100x	

Master PCH	Slave Device						
PCH_SMB_CLK PCH_SMB_DAT	JDIMM1 SO-DIMM 0x 1010 000x	JDIMM2 SO-DIMM 0x 1010 001x	JDIMM3 SO-DIMM 0x 1010 010x	JDIMM4 SO-DIMM 0x 1010 011x	JTP-1 Touch Pad 0x 2C	PJ402 uP1814A 0x 62	XDP
EC_SMB_CLK1 EC_SMB_DAT1	U5 EC						

I2C Table

Master PCH	Slave Device
PCH_I2C_CLK0 PCH_I2C_DATA0	U8 AMP TAS5766 0x 1001 100x
PCH_I2C_CLK1 PCH_I2C_DATA1	U19 LC
PCH_I2C_CLK1 PCH_I2C_DATA1	U5 EC

Flexible I/O Configuration				
I/O	High Speed Signals	Configuration	DEVICE	OCx #
Port 1	USB3 1 Capable of OTG	USB3.0	JUSB3(IO)	
Port 2	USB2 3 / SSIC 1	NC		
Port 3	USB3 3 / SSIC 2	USB3.0	JUSB2	USB_OC1_N
Port 4	USB3 4	NC		
Port 5	USB3 5	NC		
Port 6	USB3 6	USB3.0	JUSB4(IO)	

Flexible I/O Configuration				
I/O	High Speed Signals	Configuration	DEVICE	GEN
Port 7	USB3_7 / PCIE 1	AR (L0)		
Port 8	USB3_8 / PCIE 2	AR (L1)		
Port 9	USB3_9 / PCIE 3	AR (L2)	U2005 (Intel AR DP)	
Port 10	USB3_10 / PCIE 4	AR (L3)		
Port 11	PCIE 5	NC		
Port 12	PCIE 6	Card Reader	U3001	PCIE 1x Gen2
Port 13	PCIE 7	WLAN	JWLAN1	PCIE 1x Gen2
Port 14	PCIE 8	LAN	U6	PCIE1x Gen1


Flexible I/O Configuration				
I/O	High Speed Signals	Configuration	DEVICE	GEN
Port 15	SATA 0A / PCIE 9	M.2 SSD2 (L0) / SATA0		
Port 16	SATA 1A / PCIE 10	M.2 SSD2 (L1)		
Port 17	SATA 1A / PCIE 11	M.2 SSD2 (L2)	JSSD2	PCIE 4x Gen 3 /SATA Gen 3
Port 18	SATA 1A / PCIE 12	M.2 SSD2 (L3)		
Port 19	SATA 0B / PCIE 13	M.2 SSD12(L0)		
Port 20	SATA 1B / PCIE 14	M.2 SSD1 (L1)		
Port 21	SATA 2 / PCIE 15	M.2 SSD1 (L2)	JSSD1	PCIE 4 x Gen 3
Port 22	SATA 3 / PCIE 16	M.2 SSD1 (L3)		
Port 23	SATA 4 / PCIE 17	SATA HDD	U14	SATA Gen 3
Port 24	SATA 5 / PCIE 18	NC		
Port 25	SATA6 / PCIE 19	NC		
Port 26	SATA7 / PCIE 20	NC		

BOM Structure Table

BTO Item	BOM Structure
Unpop	@
CPU Option	H44e@, H42@
GPU Option	SLI@
Connector	ME@

BOARD ID Table

USB2.0 Configuration		
USB2 #	Assignment	OCx #
USB2 1	JUSB3(IO DB)	USB_OC0_N
USB2 2	JUSB2	USB_OC1_N
USB2 3	HD camera	
USB2 4	KB	
USB2 5	BT	
USB2 6	JUSB4(IO DB)	USB_OC3_N
USB2 7	NC	
USB2 8	NC	
USB2 9	Finger print	
USB2 10	NC	
USB2 11	NC	
USB2 12	NC	
USB2 13	NC	
USB2 14	NC	

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File CONFIGURATION

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B				B
A				A

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